ORIGINAL ARTICLE

Open Access

A 12-bit, low-voltage, nanoampere-based, ultralow-power, ultralow-glitch current-steering DAC for HDTV

Seyed Javad Azhari[1*], Khalil Monfaredi[2] and Salar Amiri[1]

Abstract

In this paper, a novel 12-bit current-steering binary-weighted digital-to-analog converter (DAC) based on nanoampere bits is designed and modified for high-definition television (HDTV) applications. As a part of a widely used consumer appliance, it is aimed to be such designed to consume power as low as possible. Hence, as a distinguished idea, prime concentration is focused on the reduction of the currents providing the bits of the proposed DAC. To do this, current mirrors operating in the weak inversion region are arranged to establish the least significant bit (LSB) current as low as 10 nA while the power supply is also reduced to 1 V, resulting to an ultralow power of 52.9 μW. Many other powerful ideas are then deliberately combined to maintain both high speed and very low glitches required for HDTV application despite those ultralow currents and power. The result is a speed of 100 MS/s, an ultralow glitch of ≃10.91 fAs, $|INL| \leq 0.988$ LSB, $|DNL| \leq 0.99$ LSB, and a spurious-free dynamic range of ≃73 dB. These results caused the proposed DAC to execute a distinguished overall performance (defined as figure of merit) greatly better than some other advanced ones by outstanding ratios of 77 to 277,185. Hspice simulations with the SMIC 0.18-μm complementary metal-oxide semiconductor technology have been used to validate the proposed circuit. Performance evaluation of the proposed DAC versus Monte Carlo simulations and also a wide range of temperature variations proved both its well mismatch insensitivity and thermal stability.

Keywords: DAC, Nanoampere, Weak inversion, Ultralow power, Ultralow glitch, Low voltage

Background

The digital-to-analog converter (DAC), and its different sub-blocks, is one of the most essential mixed-mode electronic building blocks which have been increasingly investigated during the last decades [1,2]. Complementary metal-oxide semiconductor (CMOS) video DACs with low voltage, high speed, and high resolution are required to enhance video quality and also to ensure feasibility of various video effects. This requires more complicated video systems which must incorporate high-speed signal processors. Especially in high-definition television (HDTV) applications, DACs of more than 10 bits in resolution and faster than 80 MHz in speed are needed [1].

A current-steering structure is usually preferred for HDTV applications. This is mainly because the current-steering structure has favorable speed, resolution, and power consumption specifications in comparison to other structures.

High-speed and high-resolution data converter design becomes more complicated when lower supply voltages and lower powers are intended. In DACs operating at lower frequencies, low output impedance and current source mismatch degrade DAC's linearity, while in evaluating the performance of high-speed, high-resolution DACs, spurious-free dynamic range (SFDR) is usually taken into account. SFDR is generally limited by charge feedthrough, glitches, or spikes which occur at major carries over certain points (0.25, 0.5, 0.75, and 1 of full scale) and also power supply noise [2].

For unary current-steering DACs, differential nonlinearity (DNL) and glitch are lower than those for binary

* Correspondence: azhari@iust.ac.ir
[1]Electronics Research Center and Electronics Department, Iran University of Science and Technology (IUST), Narmak, Tehran 1684613114, Islamic Republic of Iran
Full list of author information is available at the end of the article

Springer

ones, but in this paper, the binary structure is selected because of its simplicity, lower power consumption, and higher speed. So far, power reduction techniques mostly concentrate on reduction of voltages, but the extent of voltage reduction is narrow and cannot result to noticeable power reduction. Meanwhile, the current can be reduced to nanovalues and beyond (femto and atto) [3,4], promising extra significant reduction in power down to nanowatts and less [5]. These methods thus deserve much more approach as such in this paper. In this paper, for further power reduction, as a start, a current mirror system operating partly in the weak inversion region is adopted to provide nanocurrents accompanied with lower power supplies [6].

Altogether, the deliberately novel engineering of many powerful ideas like the aforementioned novel nanocurrent arrays, nanocurrent cells, complementary transmission gate switches, deglitchers, charge removal schemes, and latch circuits resulted to a novel ultralow-power rather glitchless 12-bit DAC whose overall structure and performance is discussed in the 'Overall structure and performance of DAC' section. The simulation results are provided in the 'Results and discussion' section, and finally, the 'Conclusions' section concludes the work.

Methods
Overall structure and performance of DAC
Figures 1 and 2 show the overall block diagram and the transistor level configuration of the proposed DAC, respectively. The proposed DAC comprises an input buffer, latch circuit, bias circuit, current source arrays, current cells, and output load.

In the following, important parts of the proposed DAC are explained in detail.

Bias circuit and nanocurrent source arrays
One of the main objectives in this work is to reduce the power consumption of the DAC. Power saving is usually achieved by reducing the supply voltage. While supply voltage reduction is currently limited to some tenths of volts, favorably, circuits operating with currents as low as femtoamperes are reported so far [3-8]. Comparing limited supply voltage reduction capability with the

remarkably large reduction factor obtainable for the currents, it is concluded that by reducing the circuit's currents, much smaller power consumption can be achieved. Therefore, the current reduction approach promises extra significant power-saving orders.

To have a sufficiently secure start, in this work, we aimed at currents in the range of nanoamperes for the binary-weighted current-steering DAC: from 10 nA for the least significant bit (LSB) leading to 20.48 μA for the most significant bit (MSB; 12 bits) while the supply voltage is also reduced to 1 V. The output impedance of the current cells needs to have an acceptable minimum value to reduce distortion in the system. To avoid the effect of the output impedance of current cells on the current delivered to the load impedance, we selected the latter which is much smaller than the former. It is worth noting that the greatest (worst) effect of the output impedance of current cells is when the digital code includes many 1's (11...11). In this condition, many current cells, which lie parallel to each other minimizing equivalent output impedance, are used to produce the desirable output current [9]. As a result, load impedance must be selected small enough [2,10-13]. On the other hand, taking impedance matching into consideration in video applications, we selected a load impedance of 75 Ω.

Consequently, biasing circuit, nanocurrent source arrays, and nanocurrent cells, which altogether are responsible to provide binary-weighted currents, play a major role in the design of this DAC [14,15]. Adopted self-biasing current source block and current arrays are shown in Figure 2. MCS1 and MCS2 transistors force the current to flow through MCS3 and MCS4. Neglecting the output resistance of MOSFET transistors and their body effect, the product of this current and the resistance of R_{CS} is equal to the gate-source voltage of MCS4. It can be seen that the current is independent of the power supply voltages and is almost constant. The constant current flowing through the MCS2 transistor makes it possible to produce different currents by the proposed current array topology. Current mirrors operate either in strong or weak inversion regions for which the following equations are presented.
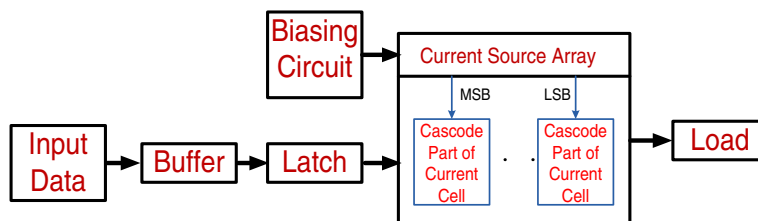

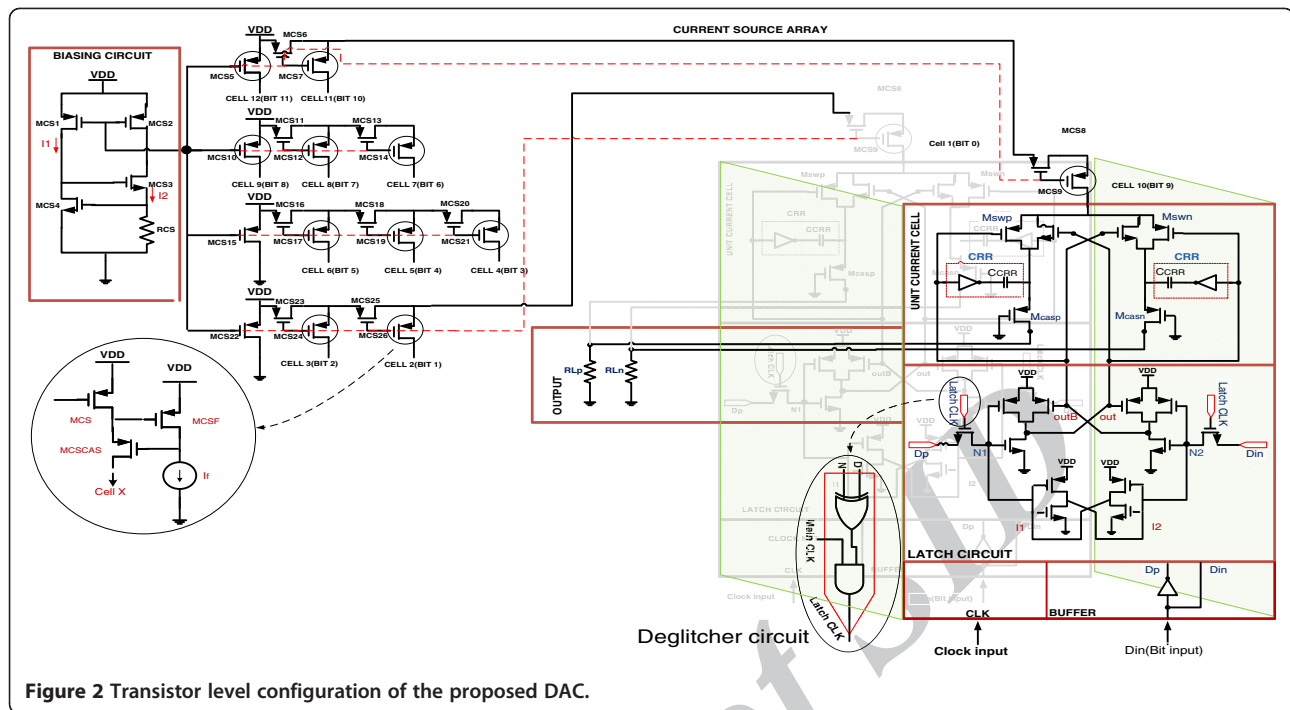**Figure 1 Overall block diagram of the proposed DAC.**

Figure 2 Transistor level configuration of the proposed DAC.

The current equation in the strong inversion region is given by Equation 1:

$$I_1 = I_2 = \frac{V_{GS4}}{R_{CS}} = \frac{V_{th} + \sqrt{2I_1/\mu_n C_{ox}(W/L)_4}}{R_{CS}} \qquad (1)$$

The current equation in the weak inversion region [10] is given by Equation 2:

$$I_{D:sub-threshold} = I_o \exp\left(\frac{V_{GS} - V_T}{nV_{th}}\right)\left(1 - \exp\left(\frac{-V_{DS}}{V_{th}}\right)\right), \qquad (2)$$

where

$$I_{D:sub-threshold}\Big|_{V_{GS}=V_{th}} = I_o = \mu_o C_{ox}\frac{W}{L}(n-1)V_{th}^2,$$

$$n = 1 + \frac{C_d}{C_{ox}},\ V_{th} = \frac{kT}{q}. \qquad (3)$$

The produced current values must be in the order of $2^n \times I_{LSB}$, where '*n*' can take the values 0, 1,..., 11 for the 12-bit DAC. These currents can be produced by modifying the aspect ratios of current mirror transistors. Hspice simulations verify that current mirrors operate in the weak inversion region for currents lower than 50 nA. The control word which is provided by the digital input makes the currents from each cell to be provided at the output load, yielding an analog current signal that is proportional to its digital origin.

The performance of just a simple current mirror is inadequate for high-performance systems like DACs. Since the overall performance of any system is limited by the performance of its subsystems, to build a high-performance DAC, a regulated cascode current mirror with high output resistance is used instead of simple current mirrors. The detailed circuit of this current mirror is highlighted in a circle in Figure 2.

To provide required currents ranging from LSB to MSB values, the current divider arrays shown in Figure 2 are used. The main advantage of using transistors in the divider instead of resistors is that they occupy less chip area and consume less power than resistors.

Current cell arrangement is very vital in the quality performance of the DAC. It could be arranged in a matrix shape ranging from 12 lines (one cell in each line) to 1 line. The more are the lines, the more will be the loading effect on the bias circuit. Otherwise, the less are the lines, the more current dividers and hence more transistors will be used. This means the more will be the occupied area and the consumed power. After a long, time-consuming deliberate try, the current source array arrangement shown in Figure 2 proved itself to be the best arrangement for the sufficiently high performance of the DAC in terms of power consumption, DNL, INL, SFDR, and output response.

Current cell

The main duty of current cells is to make currents provided by current source arrays to flow through the
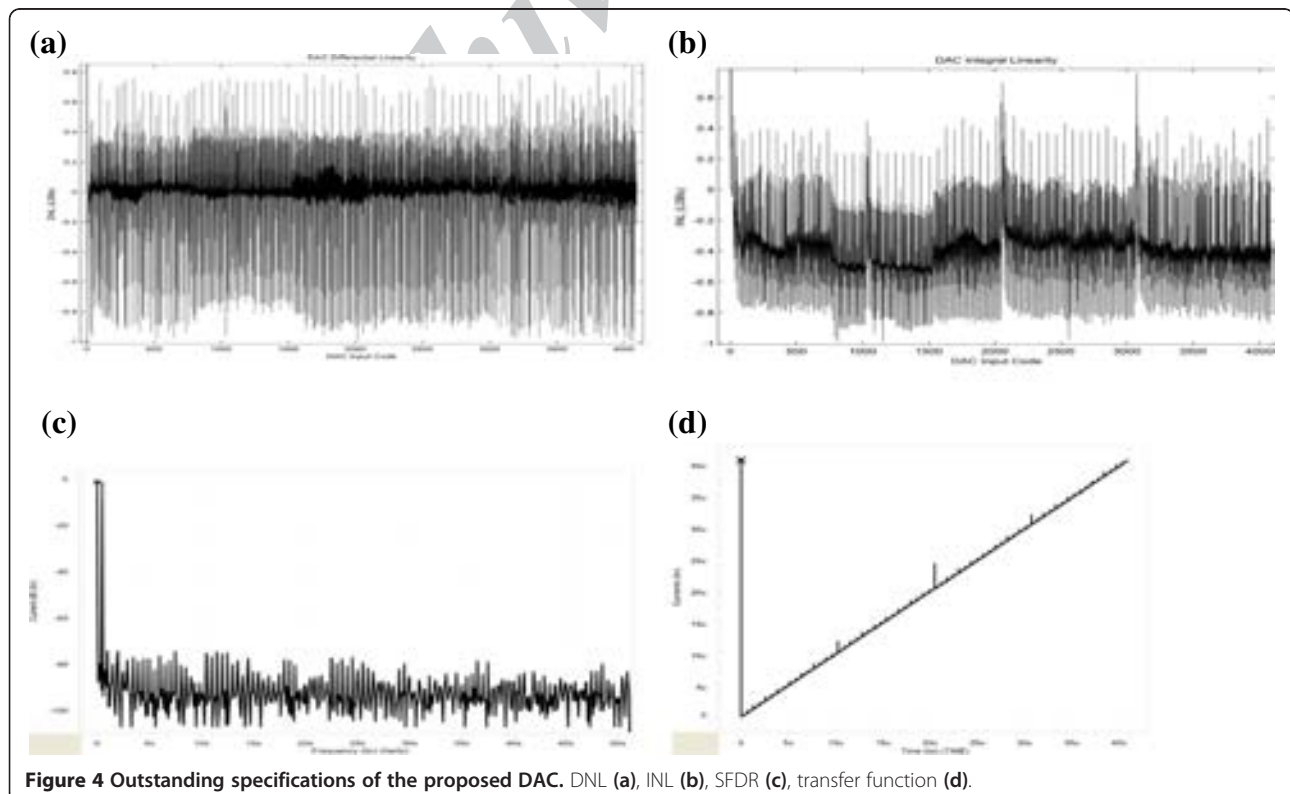
Figure 3 CRR technique.
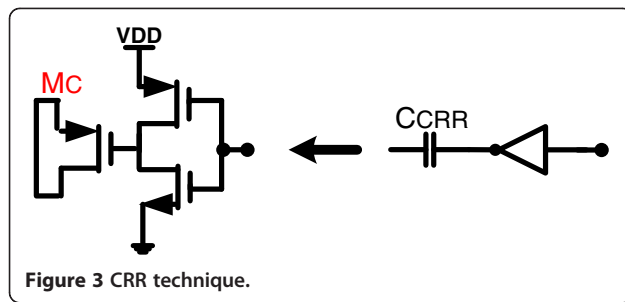
output load or not, according to the input digital data being one or zero. In order to implement each bit of DAC, one current cell is used. Cascode configuration is used in the current cell in order to increase the output impedance and reduce the sensitivity of DAC to output load variations. One important drawback which appears for nanocurrents is the glitch problem caused by clock feedthrough introduced by switching clock pulse and digital inputs. Complementary transmission gate switches as well as a deglitcher circuit are hence used to reduce the glitch and feedthrough errors by suitable aspect ratio selection. The proposed current cell is adopted from [11,12], and its modified version is shown in Figure 2 for BIT 9 (CELL 10). The deglitcher circuit compares the old and new values of the input data in each pin. If they were the same, the clock pulse will not turn the input switch on, and this means reduced glitch and clock feedthrough.

The Boolean digit and its complement provided by each digital input is latched and then applied to transmission gates conducting the available current to R_{LP} or R_{LN}. Transistors M_{CASP} and M_{CASN} are cascoded in order to make a buffer between the output load and input current. The 'charge removal replacement' (CRR) technique [12] is used in order to reduce transient time. Using this technique makes the circuit to work faster. Figure 3 illustrates the circuit responsible to do this technique where transistor M_C plays the role of the capacitor of the CRR technique (C_{CRR}). The main idea of this technique is to remove the injected positive charge due to signal switching. Furthermore, this will improve the transient characteristics by reducing the rise and fall times and makes dynamic performance better.

Latch circuit

The currents of cells are led to OUT or OUTB by the digital input value. It is, however, possible that both complementary transmission gate switches become off simultaneously. In this condition, a large amount of glitch is produced. The main idea behind the latch circuit is to modify the rise and fall times of the circuit so as to adjust the switches' off state in order not to become off at the same time [12,14-17]. For further reduction of clock feedthrough and glitch, a deglitcher circuit is used. The deglitcher circuit is shown and highlighted in an ellipse in Figure 2, in which 'Main CLK' is the
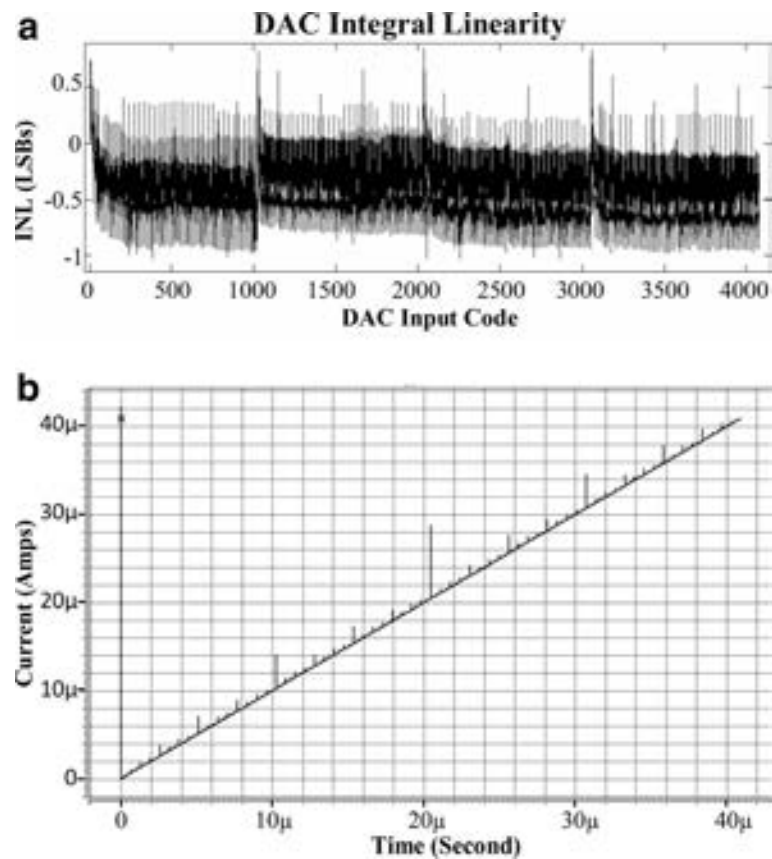

Figure 4 Outstanding specifications of the proposed DAC. DNL **(a)**, INL **(b)**, SFDR **(c)**, transfer function **(d)**.

Figure 5 Monte Carlo results of INL (a) and transfer function (b) of the proposed DAC.

Table 1 Comparative results of the proposed circuit and some other works

Specification	This work	[12]	[13]	[15]	[16]	[17]
CMOS technology	0.18 μm	0.18 μm	90 nm	0.18 μm	0.6 μm	0.35 μm
Number of bits	12	10	12	10	12	10
Sample rate (MS/s)	100	120	160	250	65	210
Supply (V)	1	1	1.3/2.6	1.8	3.3	3.3
Load (Ω)	75	200	400 differential	-	-	-
|DNL| (LSB)	≤ 0.99	Mean 0.178	≤ 0.6	≤ 0.1	0.2	0.7
|INL| (LSB)	≤ 0.98	Mean 0.134	≤ 0.6	≤ 0.1	0.8	1.1
SFDR (dB)	≥ 73	≥ 63	≥ 74	≥ 60	-	≥ 53
Glitch energy	10.914 fAs	0.4 pVs	1.9 pVs	2.64 pVs	50 pVs	76 pVs
Power (mW)	0.05294	2.5	10.6	22	71.7	83
DNL Monte Carlo (LSB)	0.96	N/A	N/A	N/A	N/A	N/A
INL Monte Carlo (LSB)	1.002	N/A	N/A	N/A	N/A	N/A
SFDR Monte Carlo (dB)	66.3	N/A	N/A	N/A	N/A	N/A
FOM (GHz/mW pVs)	9452	122.88	32.54	4.4	0.074	0.0341

N/A, not applicable.

main clock of the system, 'D' is the new value of input digit, 'N' is the latched value (i.e., the old value) of the input digit, and 'latch CLK' is the modified clock produced for each bit which is applied to the latch switch. The main idea of the deglitcher circuit is to compare the old value saved in the latch and the new one provided by the digital input. If they are the same, then the clock pulse will not be applied to the input switch. In other words, the modified clock activates the switches to latch the input digit when its value changes. Eliminating inactive inputs reduces the total glitch drastically.

Results and discussion

Using a supply voltage of 1 V, a 12-bit binary-weighted current-steering DAC of 100 megasamples (MS)/s is designed, providing currents as low as 10 nA for LSB. Hspice simulations with the SMIC 0.18-μm CMOS technology have been used which validate the high performance of the proposed circuit with outstanding specifications: ultralow power $\simeq 52.94$ μW and ultralow glitch energy $\simeq 10.914$ fAs. Its other achievements are $|INL| \leq 0.988$ LSB, $|DNL| \leq 0.99$ LSB, and SFDR $\simeq 73$ dB. The achieved DNL, INL, and SFDR of the proposed DAC are shown in Figure 4a,b,c, respectively.

For dynamic performance evaluation of DAC with simulation, a sinusoidal waveform with 500-KHz frequency is used. The SFDR achieved is higher than 73 dB which is shown in Figure 4c. The transfer function of the proposed DAC (analog output signal) is shown in Figure 4d. In Figure 4d, a few large jumps in the transfer function of the DAC can be observed that usually appear on the output signal and are known as glitch energy.

The main causes of the glitch energy are as follows:

1. Clock feedthrough caused by the switch transistor channel charge and discharge. Larger glitch amplitudes are expected for MSB due to the larger dimensions of their switches. The mid-code in the transfer function experiences relatively larger glitch energy because all bits change their states and MSB is also involved in the process of determining the new value of the output signal.
2. Unequal and asynchronous rise and fall times of current signals of different bits which change their states to build the output signal especially in binary-weighted DACs.
3. Unequal delays of different bit cells while turning 'on' or 'off' (so-called on-off jitter with the statistical nature) affected by the output signal level and different aspect ratios of switch and current buffer transistors of those cells.

Transfer function, INL, DNL, and SFDR simulation results with 4% Monte Carlo variations of both W/L and

V_{T0} yield transfer function variations less than 10%, SFDR$_{min}$ = 66.3 dB, INL$_{max}$ = 1.002 LSB, and DNL$_{max}$ = 0.96 LSB. However, to avoid lengthy discussion, only the figures of INL and transfer function are given in Figure 5a,b, respectively. The results confirm the robustness of the circuit against W/L and V_{T0} mismatches. Also, the transfer function of the proposed DAC while temperature varies from 0°C to 50°C is simulated, and transfer function variations less than 5% are achieved which tend to be a good stability factor toward temperature deviations, too. Table 1 compares some of the most important parameters of the proposed circuit with those of some other DACs. Also, to have a fair collective numerical comparison between this work and other works gathered in the table, as is used, the figure of merit (FOM) of relation (4) is defined and used. The results are recorded in the last row of the table and proved the distinguished superiorities of the overall performance of the proposed DAC in this work, ranging from 77 to 277,185 times of improvement compared to others:

$$FOM_{(GHz/mW\ pVs)} = \frac{2^N \times \text{Sample rate}}{\text{Power} \times \text{Glitch}}. \quad (4)$$

Conclusions

In this paper, a 12-bit current-steering binary-weighted DAC suitable for HDTV applications of 100 MS/s is designed. Currents as low as 10 nA for LSB and a supply voltage as low as 1 V are applied, providing such outstanding characteristics as ultralow power $\simeq 52.94$ μW, and ultralow energy glitch $\simeq 10.914$ fAs. $|INL| \leq 0.988$ LSB, $|DNL| \leq 0.99$ LSB, and SFDR $\simeq 73$ dB are the other characteristics of the proposed circuit. Hspice simulations with the SMIC 0.18-μm CMOS technology have been used to demonstrate the validation of the proposed circuit. Ultralow power consumption and ultralow glitch energy are the most outstanding achievements of this work.

Authors' contributions
SJA brought up the idea of using nanoamperes to realize ultralow-power DACs; designed the circuit; performed the study, analysis, and discussion; conducted the various simulation processes; directed the paper layout and presentation and the results to be shown and compared; corrected the English written and grammar/composition; finalized the paper; did all the revisions; and supervised the whole process of paper production. KM was the main assistant of SJA in the production process, drafted the paper, and participated in the simulations. SA performed the simulations. All authors read and approved the final manuscript.

Author details
[1]Electronics Research Center and Electronics Department, Iran University of Science and Technology (IUST), Narmak, Tehran 1684613114, Islamic Republic of Iran. [2]Electrical and Electronics Engineering Faculty, Azarbaijan Shahid Madani University, Tabriz 5375171379, Islamic Republic of Iran.

References

1. Song, M, Kang, B, Joe, E: A 10-bit 80MHZ 3V CMOS D/A converter for video applications. IEEE Trans. Consum. Electron. **43**(3), 868–872 (1997)
2. Radiom, S, Sheikholeslami, B, Aminzadeh, H, Lotfi, R: Folded-current-steering DAC: an approach to low-voltage high-speed high-resolution D/A converter. Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 4783–4786. IEEE, Washington, DC (2006)
3. Azhari, SJ, Monfaredi, K, Faraji Baghtash, H: A novel ultra low power high performance atto-ampere CMOS current mirror with enhanced bandwidth. J. Electron. Sci. Technol (JEST) **8**(3), 251–256 (2010)
4. Faraji Baghtash, H, Monfaredi, K, Azhari, SJ: A novel high performance atto-ampere current mirror. Proceedings of the IEEE International Conference on Signal Acquisition and Processing, pp. 27–30. IEEE, Washington, DC (2010)
5. Uster, M, Loeliger, T, Guggenbuhl, W, Jackel, H: Integrating ADC using a single transistor as integrator and amplifier for very low (1 fA minimum) input currents. Proceedings of the Advanced AID and DIA Conversion Techniques and Their Applications, pp. 86–89. IEEE, Washington, DC (1999)
6. Barranco, BL, Gotarredona, TS: On the design and characterization of femtoampere current-mode circuits. IEEE J. Solid State Circuits **38**(8), 1353–1363 (2003)
7. Zhang, L, Yu, Z, He, X: Circuit design and verification of on-chip femto-ampere current mode circuit using 0.18um CMOS technology. Proceedings of the 8th IEEE International Conference on Solid-State and Integrated Circuit Technology, pp. 1624–1626. IEEE, Washington, DC (2006)
8. Uster, M, Loeliger, T, Guggenbuhl, W, Jackel, H: Integrating ADC using a single transistor as integrator and amplifier for very low (1 fA minimum) input currents. Proceedings of the Third International Conference on Advanced A/D and D/A Conversion Techniques and Their Applications, pp. 86–89. IEEE, Washington, DC (1999)
9. van de Plassche, R: CMOS Integrated Analog-to-Digital and Digital-to-Analog Converter, 2nd edn. Kluwer, Dordrecht (2003)
10. Wang, A, Calhoun, BH, Chandrakasan, AP: Sub-threshold Design for Ultra Low-Power Systems. Springer, New York (2006)
11. Takakura, H, Yokoyama, M, Yamaguchi, A: A 10 bit 80 MHz glitchless CMOS D/A converter. Proceedings of the IEEE Custom Integrated Circuits Conference, pp. 26.5/1–26.5/4. IEEE, Washington, DC (1991)
12. Leong, KHA, Seng-Pan, U, Martins, RP: A 1-V 2.5-mW transient-improved current-steering DAC using charge-removal-replacement technique. Proceedings of the IEEE Asia Pacific Conference on Circuit and Systems, pp. 183–186. IEEE, Washington, DC (2006)
13. Dongwon, S, McAllister, GH: A low-spurious low-power 12-bit 160-MS/s DAC in 90-nm CMOS for baseband wireless transmitter. IEEE J. Solid State Circuits **42**, 486–495 (2007)
14. Hassanzadeh, M, Talebzadeh, J, Shoaei, O: A high-speed, current-steering digital-to-analog converter in 0.6-μm CMOS. Proceedings of the 9th International Conference on Electronics, Circuits and Systems, vol. 1, pp. 9–12. IEEE, Washington, DC (2002)
15. Deveugele, J, Steyaert, MSJ: A 10 bit 250-MS/s binary-weighted current-steering DAC. IEEE J. Solid State Circuits **41**(2), 320–329 (2006)
16. Ryu, KH, Yoon, KS, Min, HK: Design of a 3.3 V 12 bit CMOS D/A converter with a high linearity. Proceedings of the 1998 Midwest Symposium on Circuits and Systems, pp. 538–541. IEEE, Washington, DC (1998)
17. Cho, HH, Park, CY, Yune, GS, Yoon, KS: A 10-bit 210MHz CMOS D/A converter for WLAN. IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, pp. 106–109, (2004)