

Investigation of the cutoff frequency of double linear halo lightly doped drain and source CNTFET

Mohammad Javad Hejazifar · Seyed Ali Sedigh Ziabari

Received: 12 February 2014 / Accepted: 2 August 2014 / Published online: 26 August 2014
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Abstract In this work we investigate the n-type single halo implantation in channel of lightly doped drain and source CNTFET (SH-LDDS-CNTFET) and propose the n-type double linear halo implantation in the channel of LDDS-CNTFET. These transistors are simulated with a non-equilibrium Green's function method. We demonstrate that in the proposed structure the f_T at the V_{GS} ranges of 0–0.25 V and more than 0.42 V is much higher compared to the LDDS-CNTFET and SH-LDDS-CNTFET and the SH-LDDS-CNTFET, respectively. Finally, simulations demonstrate that the f_T of the proposed transistor is more than the LDDS-CNTFET at a wide range of V_{GS} , whereas the f_T of SH-LDDS-CNTFET is more than the LDDS-CNTFET for narrow ranges of V_{GS} .

Keywords Carbon nanotube field effect transistor (CNTFET) · Cutoff frequency (f_T) · Single halo (SH) · Double linear halo (DLH) · Non-equilibrium Green's function (NEGF)

Introduction

After discovering the carbon nanotube (CNT) by Ajijima [1], scientific researches about this structure are expanded due to its excellent electronic properties. One of the important properties of this structure is quasi-ballistic transport with very high carrier mobility [2, 3]. Using carbon nanotube, two types of field effect transistors have been discussed. The first type is Schottky barrier carbon nanotube field effect transistor (SB-CNTFET) and second type is MOSFET-like CNTFETs (MOSCNTs). The MOSCNT was more favorable because of the high on–off current ratio, but leakage current (I_L) of this transistor is very high because of electron band-to-band tunneling (BTBT) [4]. In order to deal with this problem, some solutions such as drain and source with a linearly or lightly doped, source and drain extensions and asymmetric oxide thickness, have been proposed [5–9]. Also, the dual material gate structure and the source and drain parameters effect on the characteristics of CNTFET are investigated [10, 11]. Moreover the p-type halo implanted deteriorates the cutoff frequency and the switching delay of CNTFET [12].

This paper is mainly focused on the f_T of MOSCNT, linearly doped CNTFET (LD-CNTFET) and lightly doped drain and source CNTFET (LDDS-CNTFET), which are discussed in [7], to select a structure with the highest f_T . Moreover, we have investigated the implantation of n-type single halo in channel of LDDS-CNTFET (SH-LDDS-CNTFET) and its effects on some characteristics such as the f_T . Based on this investigation we have proposed implanting n-type double linear halo in the channel of LDDS-CNTFET which is named “DLH-LDDS-CNTFET”. These structure characteristics such as the leakage current, the on-current and the f_T have been investigated. We have used a non-equilibrium Green's function (NEGF) method to simulate these transistors [8, 13–17].

M. J. Hejazifar
Department of Electrical Engineering, Guilan Science and Research Branch, Islamic Azad University, Guilan, Iran
e-mail: mohammad.j.hej@gmail.com

S. A. Sedigh Ziabari (✉)
Department of Electrical Engineering, Roudbar Branch, Islamic Azad University, Roudbar, Iran
e-mail: sedigh@iauroudbar.ac.ir

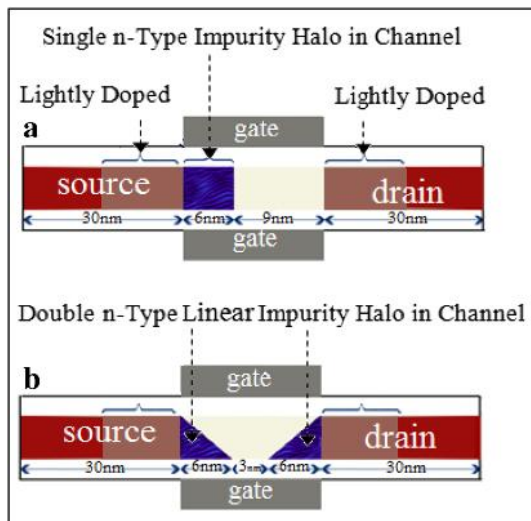


Fig. 1 The device cross-section representation. The device cross-section with implanting the n-type halo in the channel, **a** single halo and **b** double linear halo

Proposed transistor and method of simulation

A cross-section schematic representation of implanting the n-type single halo in the source side of channel of LDDS-CNTFET and their geometric details is shown in Fig. 1a. The channel is a (16, 0) CNT and radius 0.63 nm that is embedded in cylindrical gate insulator of HfO_2 with thickness 2 nm and dielectric constant 16. The channel length is 15 nm, which consists of 9 nm undoped CNT and 6 nm n-type doped CNT. The concentration of this single halo is 1.4 nm^{-1} . Our proposed structure is shown in Fig. 1b. This figure illustrates a cross-section schematic representation of the n-type double linear halo implantation in the channel of LDDS-CNTFET (DLH-LDDS-CNTFET) and their detailed geometries. The drain and source length are 30 nm, which consists of 15 nm highly doped regions and 15 nm lightly doped regions are taken to be 2 and 0.2 nm^{-1} , respectively. Figure 1b also shows that the concentration of n-type double linear halo vary from 1.4 nm^{-1} to 0 in length of 6 nm.

Self consistent solution of the Poisson and Schrodinger equations has been done within the NEGF formalism for simulating the device characteristics. The band structure of CNT is calculated by the tight-binding method with one orbital. The electrostatic potential of CNT required for calculating the Hamiltonian of Schrodinger is provided by solving the Poisson equation. By solving the Schrodinger equation, the density of states and the charge of the CNT are calculated. The Poisson equation is solved based on the charge and consequently the new potential is calculated. The iteration between the Poisson and the Schrodinger

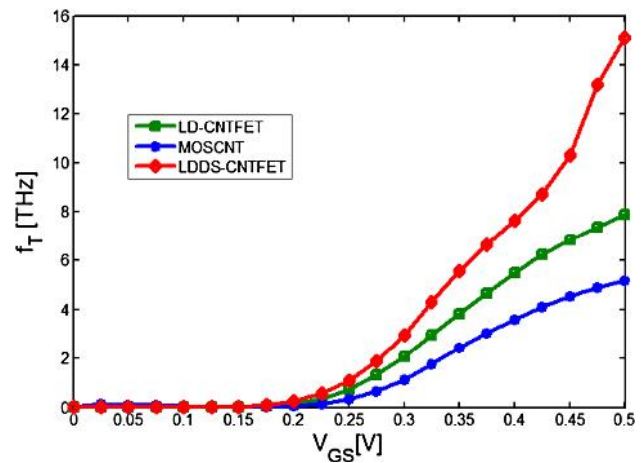


Fig. 2 The gate-source bias dependence of f_T . The gate-source bias dependence of f_T at $V_{DS} = 0.4 \text{ V}$ for MOSCNT, LD-CNTFET and LDDS-NTFET

equations stops after reaching minimum of error [6–8, 16, 17].

Results and discussion

At first, we calculate the f_T versus V_{GS} for the three structures MOSCNT, LD-CNTFET and LDDS-CNTFET as discussed in [7], to select a structure with the highest cutoff frequency. Note that these three devices have intrinsic channel. The gate capacitance (C_g) and the transconductance (g_m) are defined by [18, 19].

$$C_g = \partial Q_{ch} / \partial V_{GS}, \quad (1)$$

$$g_m = \partial I_{DS} / \partial V_{GS}, \quad (2)$$

where Q_{ch} is the total charge of the CNT channel which can be obtained by integrating over the electron density [$n(x)$] in the channel. The I_{DS} is the drain-source current. We compute the cutoff frequency using [20]:

$$f_T = g_m / 2\pi C_g \quad (3)$$

Figure 2 illustrates the f_T of MOSCNT, LD-CNTFET and LDDS-CNTFET versus V_{GS} at drain-source voltage $V_{DS} = 0.4 \text{ V}$. In comparison with the MOSCNT and the LD-CNTFET, the LDDS-CNTFET has illustrated a larger f_T . From an analytical standpoint, the doping profile of drain and source of this device leads to increase of the g_m and decrease of the channel charge variation versus gate-source voltage (C_g) and as a result, increasing the f_T -characteristic. Therefore, we choose the LDDS-CNTFET for implanting the n-type impurity halo in the channel.

We have calculated I_{DS} versus V_{GS} characteristics of the LDDS-CNTFET, the SH-LDDS-CNTFET of Fig. 1a and

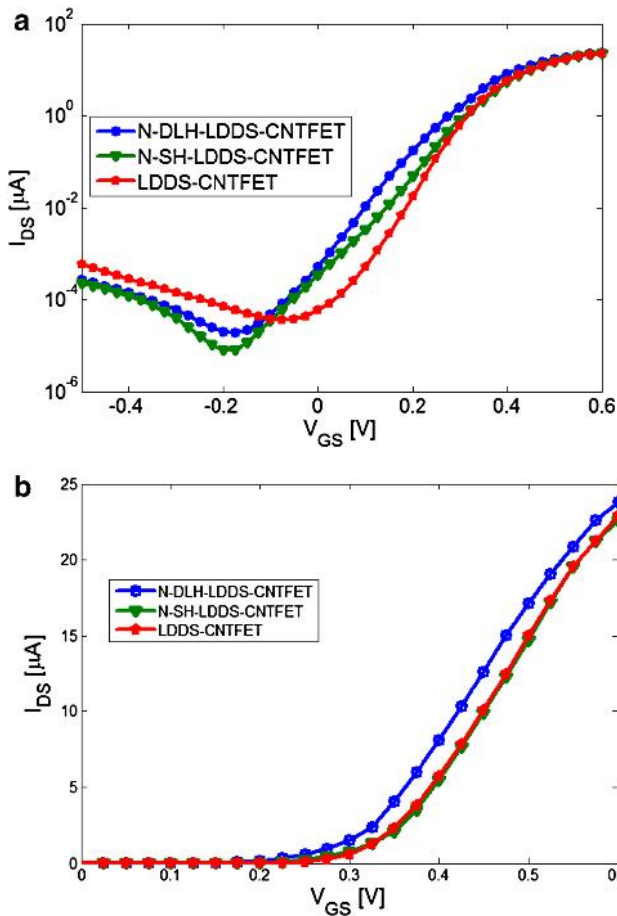


Fig. 3 The I_{DS} - V_{GS} characteristics of LDDs-CNTFET, SH-LDDs-CNTFET and DLH-LDDs-CNTFET. Comparison of the I_{DS} - V_{GS} characteristics between LDDs-CNTFET, SH-LDDs-CNTFET and DLH-LDDs-CNTFET **a** logarithmic scale and **b** linear scale at $V_{DS} = 0.4$ V

the proposed structure (DLH-LDDs-CNTFET) of Fig. 1b at $V_{DS} = 0.4$ V that are shown in Fig. 3. This figure illustrates the on-current of DLH-LDDs-CNTFET is higher than others, because the channel barrier potential of this structure is reduced by implantation of the n-type double linear halo. This figure also demonstrates that the I_L of proposed device has slightly increased when compared with the SH-LDDs-CNTFET, but it is also much less than the I_L of LDDs-CNTFET. Now we must investigate the band to band tunneling to analyze leakage current variations of these three devices.

Figure 4 shows the energy band structures (solid line) and color-scaled plot for the number of electrons per unit energy for three discussed transistors at $V_{DS} = 0.4$ V and $V_{GS} = -0.4$ V. Figure 4a illustrates a large number of tunneling electrons that causes increase the leakage current, for the LDDs-CNTFET represented in Ref. [7]. Figure 4b shows the n-type impurity halo implanted in

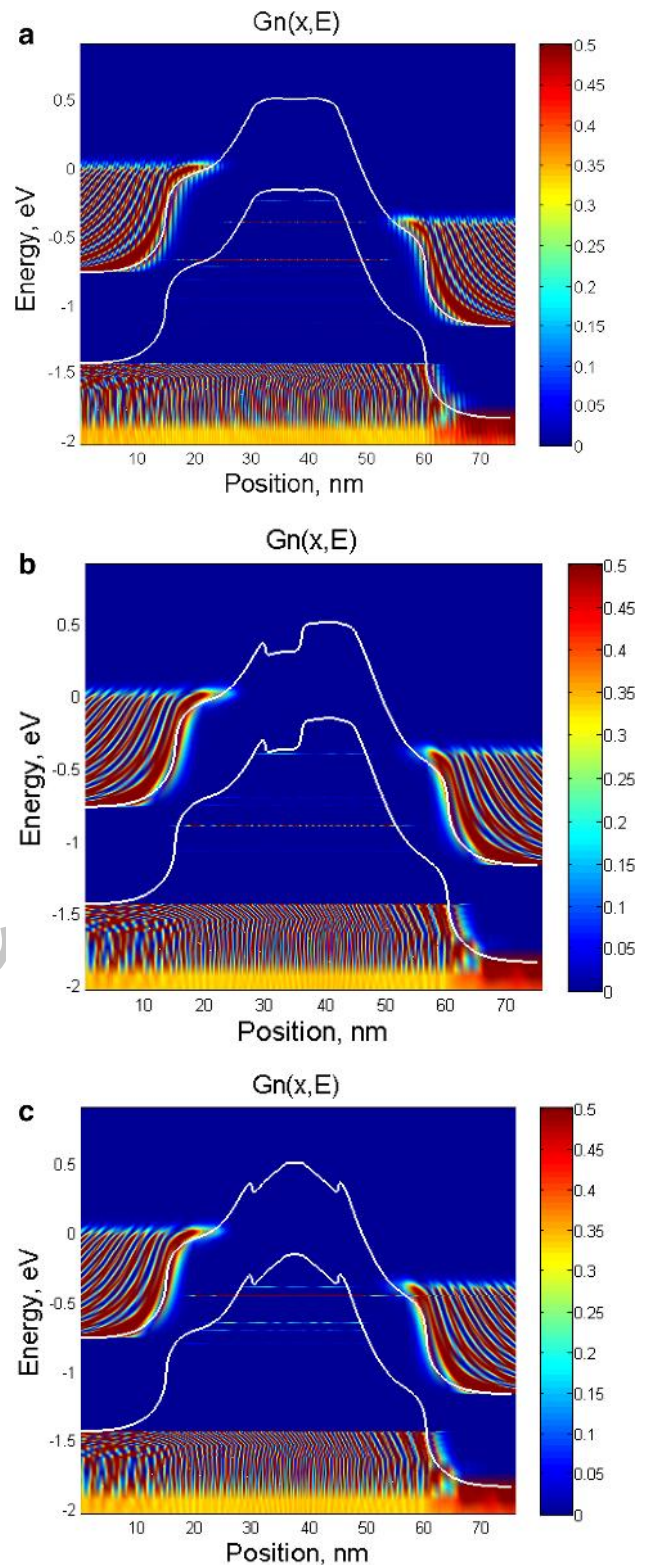


Fig. 4 The energy band structures and color-scaled plot for the number of electrons. The energy band structures (solid line) and color-scaled plot for the number of electrons per unit energy along the CNT axis for **a** LDDs-CNTFET, **b** SH-LDDs-CNTFET, and **c** DLH-LDDs-CNTFET for $V_{GS} = -0.4$ V and $V_{DS} = 0.4$ V

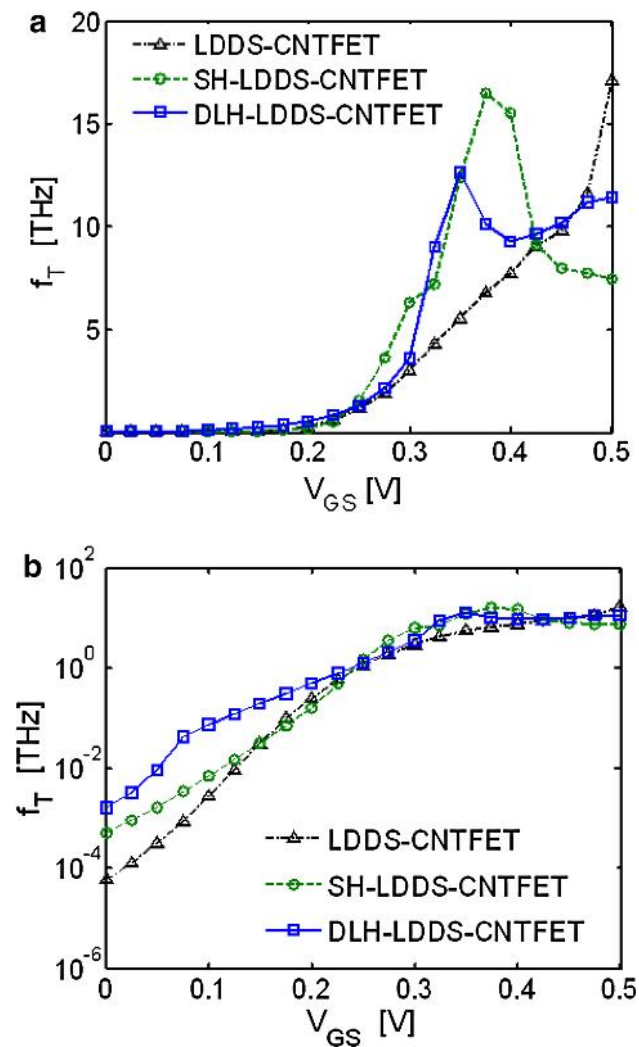


Fig. 5 The cutoff frequency versus V_{GS} for LDSS-CNTFET, SH-LDSS-CNTFET and DLH-LDSS-CNTFET. The cutoff frequency versus V_{GS} at $V_{DS} = 0.4$ V for LDSS-CNTFET, SH-LDSS-CNTFET and DLH-LDSS-CNTFET **a** linear scale and **b** logarithmic scale

channel significantly decrease the probability of electrons tunneling, because the halo causes change answers of Schrodinger equation using create the nonuniform potential. Also Fig. 4c indicates that the number of tunneling electrons in double linear halo implanted channel is a little more than the single halo structure (Fig. 4b), but much less than the intrinsic channel structure (Fig. 4a).

Then, we have calculated the f_T for the LDSS-CNTFET, the SH-LDSS-CNTFET of Fig. 1a and our proposed structure of Fig. 1b biased under $V_{DS} = 0.4$ V. These results are indicated in Fig. 5. Dash-dotted, dashed and solid lines represent the f_T for the LDSS-CNTFET, SH-LDSS-CNTFET, and DLH-LDSS-CNTFET, respectively. It can be seen in this figure that n-type single halo implant in the channel of LDSS-CNTFET increases the f_T at V_{GS} ranges of 0–0.15 V and 0.22–0.42 V. The reason of

increasing the f_T increases the transconductance. This figure also demonstrates that the cutoff frequency of DLH-LDSS-CNTFET significantly increases at low V_{GS} range ($V_{GS} = 0$ –0.25 V). From an analytical standpoint, using double linear halo the sensitivity of channel charge versus the V_{GS} variations (C_g) is decreased, therefore according to (3) this device cutoff frequency is increased. As well, the cutoff frequency of the proposed device in the V_{GS} higher than 0.42 V is more than the single halo structure. On the other hand, the cutoff frequency of DLH-LDSS-CNTFET (solid line) is more than the LDSS-CNTFET (dash-dot line) in the wide range of the V_{GS} from 0 to 0.47 V, In that event the cutoff frequency of single halo structure (dash line) is more than the LDSS-CNTFET in the V_{GS} regions of 0–0.15 V and 0.22–0.42 V. Finally, we have simulated the cutoff frequency of LDSS-CNTFET with implanting p-type single halo in the channel. Our results show that this parameter decreases strongly.

Conclusion

In this paper, we have demonstrated that the cutoff frequency of LDSS-CNTFET is higher in comparison with those of both the LD-CNTFET and the MOSCNT. We have simulated these devices by non-equilibrium Green's function method. It can be seen that in the n-type single halo structure the leakage current is significantly decreased and the f_T in the gate voltage ranges of 0–0.15 V and 0.22–0.42 V is increased. We have realized that the f_T of the proposed transistor (Fig. 1b) for V_{GS} of 0–0.25 V is much higher than either the LDSS-CNTFET or the SH-LDSS-CNTFET. And also the f_T of the DLH-LDSS-CNTFET is higher than the SH-LDSS-CNTFET for V_{GS} higher than 0.42 V. Moreover, we have illustrated that the f_T of the proposed device is higher than the LDSS-CNTFET for a broad range of V_{GS} which means 0–0.47 V, whereas the f_T of SH-LDSS-CNTFET compared to the LDSS-CNTFET is superior only in the narrow ranges of gate-source voltage.

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