

Monolithic Low Power RFIC Amplifiers for Multimode Wireless Communication Applications

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Abstract: This paper deals with the design consideration and performance results for low power low noise self-matched as well as an inductive-matched SiGe amplifier developed for the GSM/DCS/WCDMA multi-band cellular systems. The self-matched amplifier is based on the current reuse concept, and accommodates an active balun. On the other hand, the inductive-matched amplifier is a single-stage common emitter circuit with inductive on-chip matching. Both amplifiers have internal bias circuits. These amplifiers consume 5.0mA and 6.0mA at 3V to respectively provide a power gain of higher than 18dB and 13dB, a noise figure lower than 4dB, and an IIP3 higher than -16dBm and -4dBm, over 0.9-2.2GHz. With such a low current consumption, the developed amplifiers can be a candidate for low-power multimode mobile terminal applications.

Keywords: Monolithic, Amplifier, SiGe, Wireless

1. INTRODUCTION

The challenges of the multimode RF front-end design are set by the standards and are related to different reception bands as shown in Table 1. The GSM operates at 900 MHz, the DCS operates at 1800 MHz, and the WCDMA operates at 2100 MHz. In addition, these systems have different channel spacing and symbol rates. In the past, multimode receivers have been realized as a multiple number of single-mode receivers thus occupying a large area and being rather costly. A direct conversion receiver (DCR) is considered as feasible architecture for multimode mobile wireless applications [1]-[9]. A DCR is

amenable to monolithic integration, provides

Table 1: Cellular system standards and specifications.

	GSM 900	DCS 1800	WCDMA
Main Application	Voice	Voice	Data
Multiple Access Method	DS-CDMA	TDMA	TDMA
Duplex Method	TDD/FDD	TDD/FDD	FDD
Modulation	GMSK (0.3 Gaussian Filter)	GMSK (0.3 Gaussian Filter)	QPSK
Base Station Receive Band [MHz]	880-915	1710-1785	1920-1980
Mobile Station Receive Band [MHz]	925-960	1805-1880	2110-2170
Channel Spacing	200 kHz	200 kHz	5 MHz
Data Rate	270.83 kbps	270.83 kbps	144 kbps/384 kbps/2 Mbps

a cost-effective receiver solution, and reduces the size and power consumption by minimizing the number of receiver components. Furthermore, an adaptable solution processes an input RF signal from different cellular systems, and so obviates the need for multiple RF hardware. This paper describes low power SiGe amplifiers for multimode DCR applications.

2. DESIGN CONSIDERATION

2.1. Self-Matched Amplifier

The schematic diagram for the LNA with an active Balun is depicted in Fig. 1. The LNA is a two-stage common-emitter amplifier with current sharing. In comparison to a two-stage common-emitter amplifier with separate bias for each stage, this configuration reduces the power consumption by one-half. Additionally, it provides a broadband input matching, low noise and output-input isolation. The size of C2 and C3 is to minimize the tradeoff between the LNA gain, third-order input intercept point (IIP3) and input matching. R2 and R3 compromise gain and linearity. The LNA takes the advantage of the Miller effect to provide input impedance matching. Therefore, since no frequency-selective matching elements are employed, relatively broader gain and input matching can be expected. C2 and C3 ensure that the load and the voltage gain of the first stage are capacitive to shift the input Miller impedance to a resistive value, which can be shown analytically.

2.2. Active Balun

Single-ended to balanced conversion is performed using a common-emitter balun (Q3) circuit, as depicted in Fig. 1. The balun is connected to the LNA output and enables the use of double-balanced mixers. It is prohibitive that the balun be the first stage, because of high noise and noise figure mismatch between the 0- and 180- degree paths.

2.3. Inductive-Matched amplifier

As shown in Fig. 2, the inductive-matched amplifier is a one-stage common-emitter amplifier with inductive degeneration for input matching. The amplifier utilizes a resistive- capacitive feedback, which sets a 50-Ohm input and output impedance at all frequencies of interest. Additionally, a 1-nH inductor is used for emitter degeneration purpose that improves the amplifier's input matching. The amplifier is biased for the class-A operation to meet linearity requirements in the GSM, DCS, and WCDMA modes.

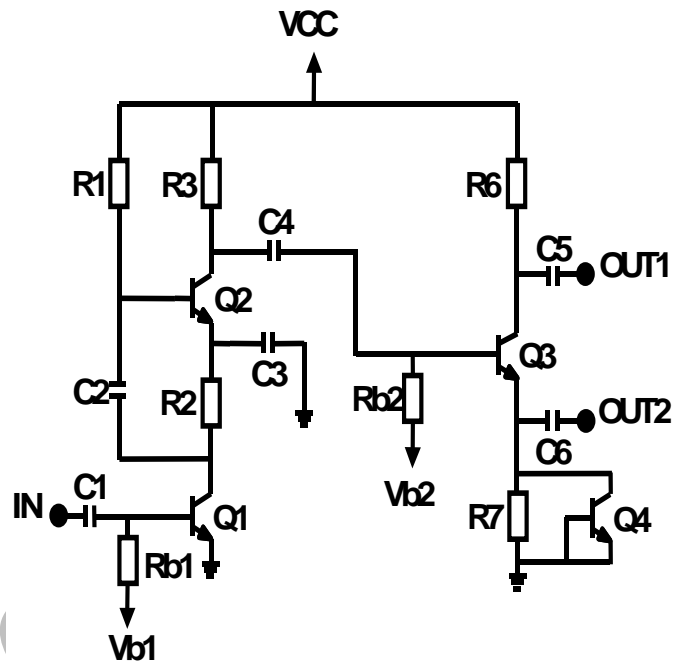


Fig. 1: Self-matched amplifier + Balun circuit.

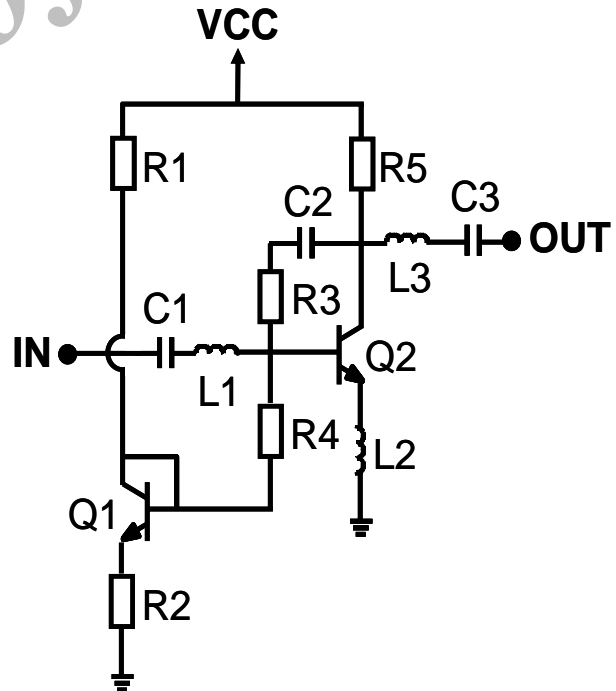


Fig. 2: Inductive-matched amplifier circuit.

2.4. Bias Circuit

All the voltages for the above amplifiers are generated on chip using both NPN and LPNP transistors in a Nagata Current Mirror structure. The

device sizes as well as the resistor values were optimized to generate a reference voltage insensitive to the variation of the bias supply voltage ripples and fabrication mismatches of over $\pm 20\%$ from the nominal values of the circuit components.

3. FABRICATION PROCESS

All the circuits were fabricated using Atmel's SiGe1 process, a 1- μm double-poly lithographic technology for RF, power and high-speed analog and digital applications. The minimum emitter size of an NPN transistor is $0.9\mu\text{m} \times 1.7\mu\text{m}$. This SiGe1 technology features NPN transistors with 50 GHz cut-off frequency and 3-V breakdown voltage, a lateral PNP transistor, ESD, Schottky, and PIN diodes, dielectric and nitride capacitors and low-, medium- and high-ohmic poly-resistors. Conventional $20\text{-}\Omega\text{cm}$, p-type substrates are used to provide low collector-substrate capacitances. The first polysilicon (p-type) layer, obtained by SiGe epitaxial deposition on the field oxide, is used for two types of polysilicon resistors (low and high-ohmic resistance), as well as for the bottom electrode of dielectric capacitors. The p-type poly 1 is used for all p+ connections (e.g. extrinsic diodes, collector and emitter of LPNP). The second polysilicon layer is an Arsenic doped alpha-silicon layer. Three types of resistors are available in the SiGe1 process: 1. low-ohmic, salicided, p-type, medium-ohmic, n-type, poly2 resistor, with $110\ \Omega/\text{sq}$ density; 2. high-ohmic, p-type, poly1 resistor, base of NPN, substrate connection, ESD and PIN poly1 resistor, which density is $4.5\ \Omega/\text{sq}$; 3. with $360\ \Omega/\text{sq}$ density. The nitride capacitor comprises a salicided poly 1 bottom electrode and a metal1 top electrode, with 67 nm nitride layer in between them. The Zener-diode for ESD is formed by an n+ buried layer below p+ substrate. Varactor diodes are typically designed as NPNs using the emitter-base junction and connecting the collector to a fixed voltage. If the voltage bias of the emitter-base diode is not sufficient, an ESD diode can be used as a varactor. NPN HBTs (Heterojunction Bipolar Transistors) are formed with self-alignment between the emitter and the base using a poly inside spacer for the minimum geometrical emitter width of $0.9\ \mu\text{m}$ and an oxide outside spacer to protect the inner transistor from the outside base implant and salicidation. Two different circularly-shaped lateral PNP transistors with current gains of 3 and 5 are available in SiGe1, as well as three metallization layers. The Metal 1 is made of Ti/TiN (180 nm), which is used as a barrier layer, and AlSiCu ($0.7\ \mu\text{m}$, $41\ \text{m}\Omega/\text{sq}$). The Metal 2 is made of AlSiCu ($1.5\ \mu\text{m}$,

$19\ \text{m}\Omega/\text{sq}$). If a third, optional metal layer is desired, the Metal 2 is covered by thick oxide and planarized by chemical-mechanical polishing (CMP). After this planarization, an additional oxide layer is deposited, followed by the Metal 3 (AlSiCu, $2.5\ \mu\text{m}$, $12\ \text{m}\Omega/\text{sq}$).

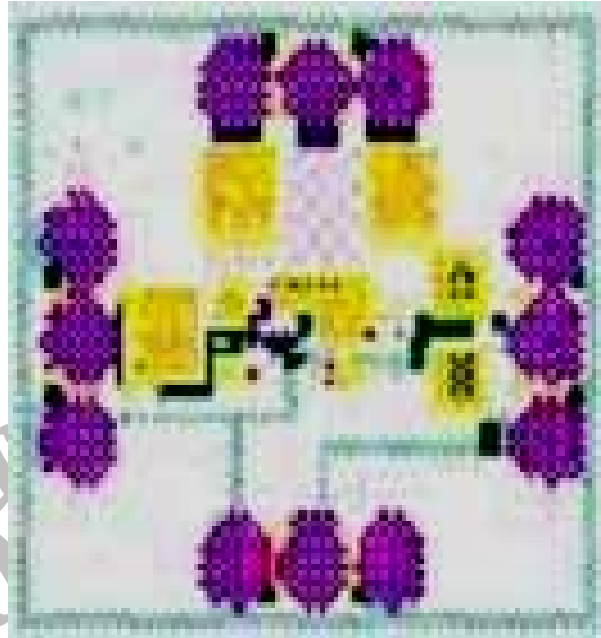


Fig. 3: Self-matched amplifier chip.

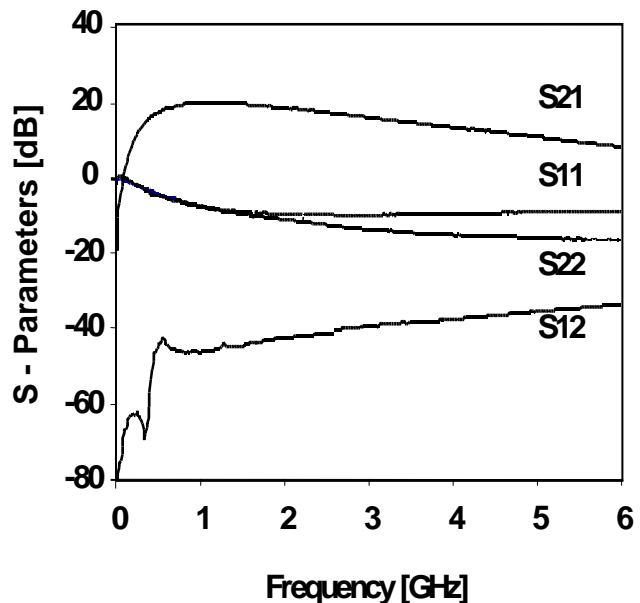


Fig. 4: Self-matched amplifier + Balun small signal S-parameters.

4. MICROWAVE PERFORMANCE

4.1. Self-Matched Amplifier and Active Balun

The self-matched amplifier chip, shown in Fig. 3, measures 0.8mm×0.67mm. Fig. 4 shows the small signal S-parameters measurement results over 6GHz.

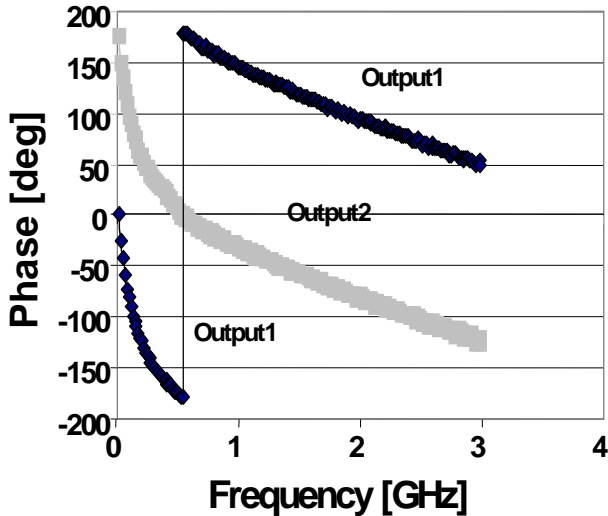


Fig. 5: Phase relation between Balun's outputs.

The combined LNA+Balun circuit's gain is 19dB at 0.9GHz and 18dB at 2.2GHz, while its noise figure is 3.0dB at 900MHz and 4.0dB at 2.2GHz. The circuit draws 5.5mA from a 3-V supply, including the bias

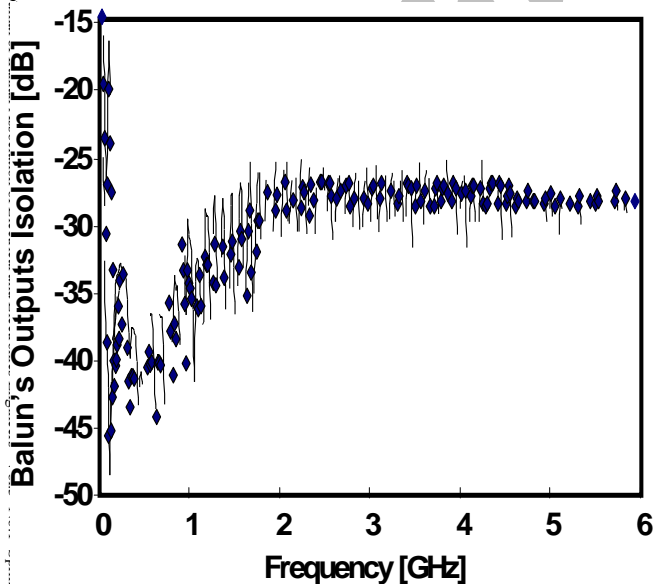


Fig. 6: Isolation between Balun's outputs.

circuit current dissipation. The input return loss is better than 9dB over 900MHz to 2.2GHz. The in-phase-output return loss is better than -15dB, whereas the out- of-phase-output return loss is better than -13dB over 900MHz to 2.2GHz. On the other hand, the measured two-tone (50kHz offset) input third order intermodulation intercept point, IIP3, of the combined LNA+Balun is about -16dBm. As shown in Figs. 5 and 6, the phase imbalance and the isolation between the Balun's complementary outputs is less than 2.5 degrees and better than 27dB, respectively. In addition, the noise figure and gain imbalance for the Balun's complementary outputs are, 0.2dB and 0.16dB, respectively, over 900MHz to 2.2GHz. The amplifier has almost a flat gain over 19dB±1.0dB over the whole GSM/DCS/WCDMA verifying the validity of the self-matching concept utilized for both the LNA circuit with reduced power consumption. Input-output isolation for the amplifier is better than 40dB.

4.2. Inductive-Matched amplifier

The inductive-matched amplifier chip, shown in Fig. 7, measures 0.8mm×0.67mm. Fig. 8 shows the small signal S-parameters measurement results over 6GHz. The amplifier circuit's gain is 13dB at 0.9GHz and 10dB at 2.2GHz, while its noise figure is 3.2dB at 900MHz and 4.2dB at 2.2GHz. The circuit draws 6mA from a 3-V supply, including the bias circuit current dissipation. The input return loss is better than -12dB over 900MHz to 2.2GHz. On the other hand, the measured two-tone (50kHz offset) input third order intermodulation intercept point, IIP3, of the amplifier is about -10dBm at 900MHz and -4dBm at 2.2GHz.

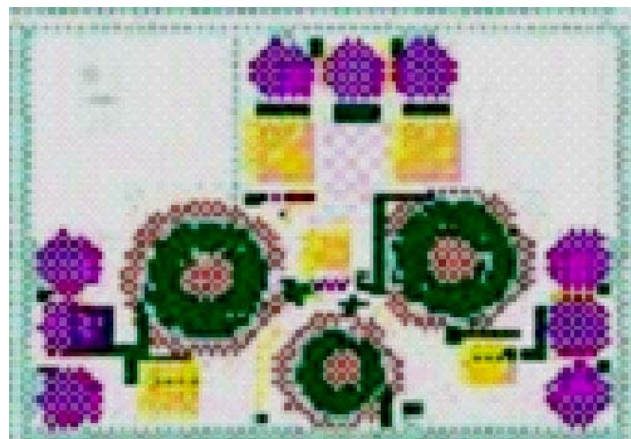


Fig. 7: Inductive-matched amplifier chip.

5. COCLUSION

Design consideration and performance results for low power SiGe amplifiers developed for the GSM/DCS/WCDMA multi-band cellular systems were described. The self-matched amplifier IC chip applies a current reuse concept to facilitate both a low power and wideband matching without using bulky on-chip inductive elements, as well as an improved IIP3. On the other hand, the inductive-matched amplifier has a one-stage common-emitter configuration with inductive degeneration and resistive-capacitive feedback to facilitate both input and output impedance matching at all frequencies of interest. These amplifiers consume 5.5mA to 6mA at 3V through on-chip bias over 900MHz to 2.2GHz. With such a low current consumption, these amplifiers are ideal for low-power multimode mobile terminal applications.

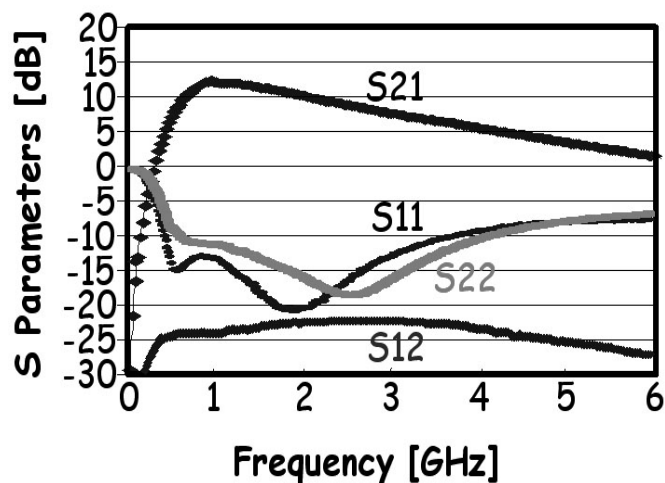


Fig. 8: Inductive-matched amplifier small signal S-parameters.

ACKNOWLEDGEMENT

The author would like to acknowledge the contribution and support from M. Kovacevic.

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