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ORIGINAL ARTICLE

Novel efficient fault-tolerant full-adder for quantum-dot cellular automata

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Abstract

Quantum-dot cellular automata (QCA) are an emerging technology and a possible alternative for semiconductor transistor based technologies. A novel fault-tolerant QCA full-adder cell is proposed: This component is simple in structure and suitable for designing fault-tolerant QCA circuits. The redundant version of QCA full-adder cell is powerful in terms of implementing robust digital functions. By considering two-dimensional arrays of QCA cells, fault tolerance properties of such block full-adder cell can be analyzed with misalignment, missing and dislocation cells. To verify the functionality of the proposed device, some physical proofs and computer simulations using QCADesigner are provided. Both simulation results and physical relations confirm our claims and its usefulness in designing fault-tolerant digital circuits.

Key words: *Design and modeling; Fault-tolerant logic gates; Full-adder; Hardware redundancy; Nanoelectronic circuits; Quantum-dot cellular automata.*

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INTRODUCTION

In recent years CMOS technology proved that it can be readily challenged by other technologies when it arrives at nano-regimes. Because of serious CMOS technology limits in nano-scales, researchers have looked into alternative technologies. Quantum-dot cellular automata (QCA) are one possible alterative technology. QCA is an emerging technology that offers a revolutionary approach and has displayed extra low power, extra high speed and extremely dense digital circuits [1, 2]. Two fundamental units of QCA based design are majority and inverter gates; so, efficient construction of QCA circuits using majority and inverter has attracted several attentions [2-23].

More recently, much work is being put into fabricating and testing molecular and magnetic QCA. Both magnetic and molecular QCA will make room temperature operation possible, which currently appears to be major SPF (single point of failure) in transitioning this technology into practice.

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When designing QCA circuits, we would like estimate power quickly in order to choose among many different alternatives. However, from a design automation point of view it is important to design for the worst case. For worst case consideration, the upper bound for power is more relevant [24]. The power dissipation for a QCA cells can be expressed as the sum of power estimates computed on a per cell basis. Each cell in a QCA circuit sees three types of events: (i) clock going from low to high so as to depolarize a cell, (ii) input or cells in previous clock zone switching states, and (iii) clock changing from high to low, latching and holding the cell state to the new state. Clock energy needs to be high to drive the cell into an intermediate, depolarized state. In a fully depolarized state, the change in driver polarization has no effect on the driven cell; hence the switching power is zero. This is the ideal case. However, to achieve this, the clocking energy needs to be high and, consequently, the associated leakage power would be high [24-30].

QCA computation does not involve electron

transfer between adjacent QCA cells. Since only few electrons are involved in QCA computations, it is susceptible to thermal issues. Therefore it is important to model and consider power as an important feature during the QCA design process along with defects [24].

A single-bit full-adder can be implemented by using only majority and inverter gates [1]. As full-adder cell is the principle element of the arithmetic systems, its performance directly affects performing the entire system. Therefore, efficiently constructing a full-adder in QCA is important [2-3, 8-10, 13-16]. Also, QCA can be used for the in-memory computing applications, which is other important issue in QCA researches [31-32].

Fault-tolerant design of QCA logic circuits is necessary for characterization of defective behavior of QCA circuits. In recent years the fault tolerance properties of QCA circuits has been demonstrated by many researchers [6-13, 33-39].

As already mentioned, full-adder cell is the basic element of QCA circuits; this note studies a new design for fault-tolerant full-adder cell that offers remarkable robustness about misalignment, missing and dislocation cells. The presented methods justified based on some physical models. Improving the robustness of the full-adders leads to efficient designing of many fault-tolerant arithmetic circuits.

EXPERIMENTAL

FAULTS AND FAULT TOLERANCE IN QCA CIRCUITS

Review of QCA

Quantum cellular automata are a new architecture, which is proper for the nanometer scale. The principle of QCA was first proposed by Lent and Tougaw [40]. The basic computational element in QCA is a quantum cell. A quantum cell can be viewed as a set of four charge dots, positioned at the corners of a square. The cell contains two extra mobile electrons, which are can quantum mechanically tunnel between dots but not cells [1, 41]. The electrons are forced to the corner positions by Columbic repulsion. The two possible polarization states represent logic "0" and "1" as shown in Fig. 1a [1, 42].

As shown in Fig. 1b, an ordinary QCA majority gate needs only five QCA cells; three inputs labeled A, B and C, the device cell and the output. The logic function of majority gate is:

$$M(A, B, C) = AB + AC + BC \quad (1)$$

As drew in Fig. 1c, each five-input majority gate must have five inputs and one output [12]. The majority voting logic function can expressed in fundamental Boolean operator as shown in

$$M(A, B, C, D, E)=ABC + ABD + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (2)$$

Also as shown in Fig. 1d, each single-bit full-adder can implement with only inverters and majority gates. The device has three inputs: two operands A, B, and the previous carry result C_{in}. The two outputs are the sum S and the carry bit C_{out}. Full-adder cells can easily chained together to produce a multi-bit adder. And in Fig. 1e a QCA inverter is shown.

As stated earlier, a QCA array performs calculation through Columbic interaction among neighboring cells that causes them to influence each other's polarization. Therefore, computation with QCA arrays is edge driven, which both energy and information flow in from the edges of the array only. This provides directionality computation by array. In this sense, the difference between input and output cells is simply that inputs are fixed while outputs are free to change [42]. The QCA array then performs the wished computation by reacting to the change in the boundary conditions. The fact the computation is edge driven implies that no direct contacts to interior cells made and thus removing the interconnection problem. This further implies the model involves computing with ground states. That is, the QCA array reacts to change in the input and settles to a new ground state, which represents solution of the needed computational problem for which the array is specifically designed. However, computing with ground state implies the estimate is temperature sensitive. In fact, if the thermal variations excite the array above its ground state then the array may produce wrong results. Besides, dynamics of array is hard to control. Thus, setting time to ground state cannot control or predict vary depending on complexity of array. Also, the array might settle to a stable state, producing wrong result or leading to a significant delay in reaching the true ground state.

To overcome these limits of computing with ground state, a switching scheme has developed [42]. In this scheme, a QCA array divided into sub-arrays and a different clock controls each sub-array. The proposed clock scheme for QCA is multi-phased. This clocking scheme allows a given sub-array to perform its computation, have its

state frozen by raising its inter-dot barriers, and then have its output as the input to the successor sub-array. Due to the multi-phase nature of this clocking scheme, the successor sub-array kept in an unpolarized state so it does not influence calculating preceding sub-array. Such clocking scheme implies a pipeline computation since different sub-array can perform different parts of the computation. In this sense, QCA arrays are inherently suitable for pipeline and systolic computation.

Advantages and Difficulties of QCA-based design

QCA offers several distinct advantages over traditional technologies: (1) This schema inherently allows for small feature size and thus high computational density. (2) Because current does not flow through QCA-based circuits, these designs can act at low power levels. This low power cost is vital to being able to achieve the device densities. (3) QCA design support massively parallel computational architectures, which can allow for more efficient information processing.

Many obstacles must be overcome before QCA-based circuits are available as a viable technology: (1) quantum cells must be small, on the order of 18nm, to be efficient. Currently the technology does not exist to make reliably quantum cells of this size and assemble them into particular structures. Fortunately much time and effort is being spent on these scale related issues. (2) Similar to any technology on this scale, difficult to create interfaces between the computational circuits and I/O devices such as monitors and keyboards that would allow the user to interact with the computer. (3) QCA structures display propagation delays. This delay can apply to finite amount of time, takes for the electrons in a cell to tunnel to their new position [5].

Faults and Fault tolerance

A fault is a physical defect, imperfection, or flaw that occurs within some hardware or software component. Fault tolerance is the ability of a system to continue to perform its tasks after to occurrence faults. The eventual goal of fault tolerance is to prevent system failures from ever occurring. Fault tolerance can achieve by many techniques.

When fault tolerance is required, some form of redundancy is also required. Redundancy is simply adding of information, resources, or time beyond

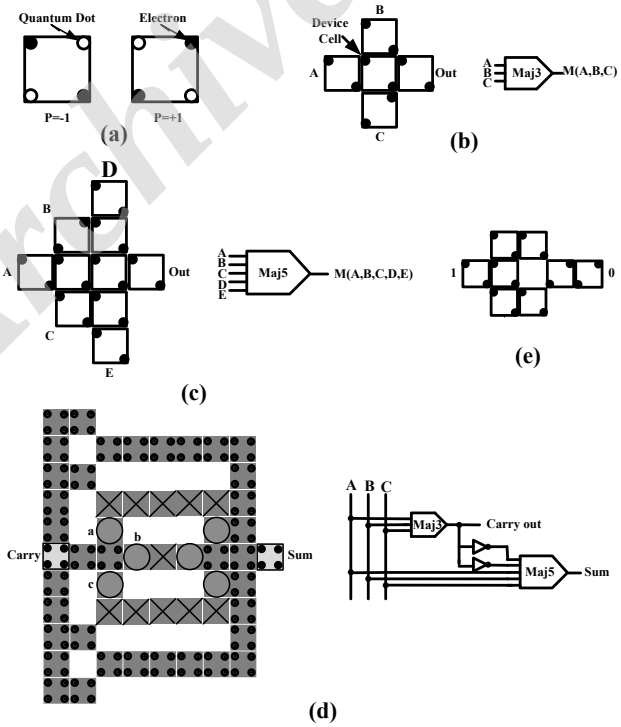

Fig. 1: (a) Basic QCA cell and binary encoding, (b) A three-input majority gate, (c) A five-input majority gate, (d) A single-bit full-adder (e) A QCA inverter.

what is needed for normal system operation [43]. In this note, we will use hardware redundancy techniques for QCA based design.

Three major categories of faults can occur during the assembly of a QCA circuit. First, faults may occur when quantum cells shifted from their intended locations which called “misalignment” cells (Fig. 2a). Sometimes misalignment cells have no effect on functionality of a QCA circuit, and sometimes they can cause a circuit to have an unexpected output. Second type of faults occurs when quantum cell “missing” resulting in the cell becoming defective and it would have no influence on its neighbors and it can cause a circuit to stop functioning well (Fig. 2b). A third type of faults occurs when quantum cells rotated about the other cells in the array which called “dislocation” cells. Also, in this case, the circuit may end to function (Fig. 2c).

Based on researches which have performed so far, some fault-tolerant QCA circuits have faults. In next section, we have tried to make a novel fault-tolerant full-adder cell using physical relation, in such a manner that it can continue to work correctly if the mentioned faults.

RESULTS AND DISCUSSIONS

Fault-tolerant full-adder

The novel proposed design for fault-tolerant full-adder shown in Fig. 3. In this new structure, a fault-tolerant full-adder can implement only with fault-tolerant majority and inverter gates. In this scheme we have three inputs labeled a, b and c and two output cells are shown by Sum

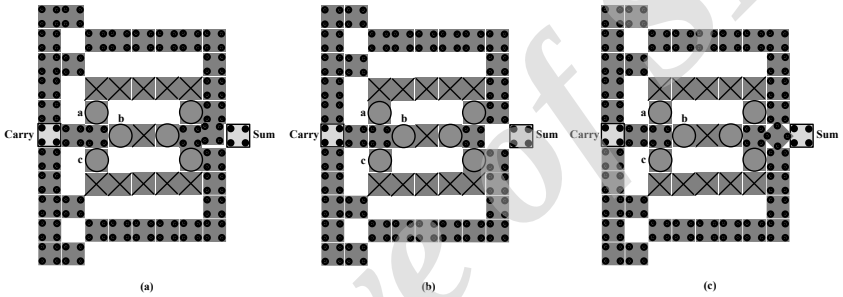

Fig. 2: Faults of single-bit full-adder, (a) misalignment cell, (b) missing cell and (c) dislocation cell.

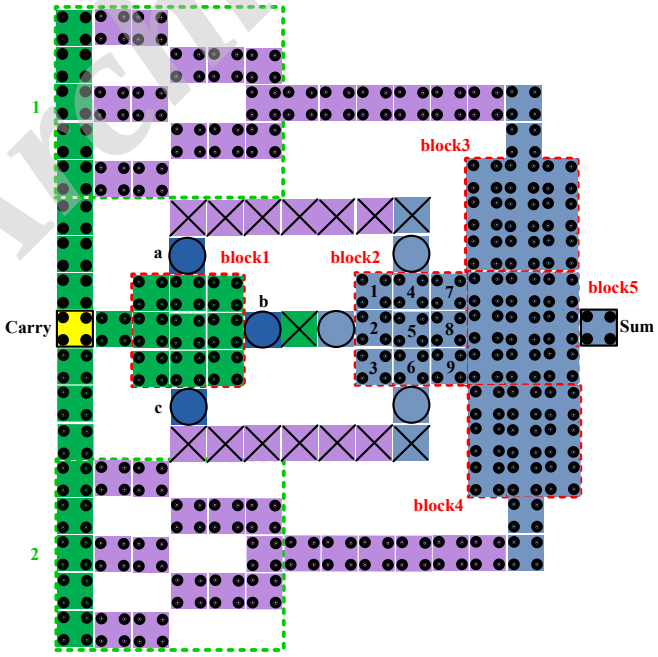

Fig. 3: Proposed fault-tolerant full-adder.

and Carry. In addition, five block 9th middle cells labeled block1, block2, block3, block4 and block5 and two block 18th middle cells labeled 1 and 2. Polarization of input cells is fixed and middle cells and output cells are free to change. The rest of cells are considered as wire.

The presented scheme is justified based on physical relations. About physical proofs, assume cells similar with length of a (a=18nm) and a space of x (x=2nm) between two neighbors.

In all figures, rectangles show a QCA cell and the circles inside show the electrons within that cell. Please note that to achieve more stability, electrons of QCA cell arrange in such a manner that reaches minimum kink energy (the difference in electrostatic energy between the two polarization states).

The kink energy between two electron charges calculated using Eq. (3a). In this equation, U is kink energy, k is fixed colon, q_1 and q_2 are electric charges and r is the distance between two electric charges. By putting the values of k and q, we earn Eq. (3b). U_T is the summation of kink energies that calculated from Eq. (4) [44].

$$U = \frac{kq_1q_2}{r} \quad (3a)$$

$$kq_1q_2 = 9*10^9*(1.6)^2*10^{-38} = 23.04*10^{-29} = A = cte \quad (3b)$$

$$U_T = \sum_{i=1}^{2} U_i \quad (4)$$

Physical Proof

As the proposed design has 81 different middle cells, we should check all the faults that may occur in middle cells to verify the correctness of this scheme. Only one of faults (missing cell 5 in block2) proved and others proved as well. The assumed value of input cells are a=b=0 and c=1.

First, we calculate the kink energy existing between each electron (e_1, e_2, e_3, e_4, e_5, e_6, e_7, e_8, e_9 and e_{10}) with electrons "x" and "y" in (a) and (b) states using (3a) and (3b) equations. For example is the kink energy existing between electrons and x (or y). Also, is the distance between two electron charges. Then we calculate the total kink energy (U_T) in both states using Eq. (4). Comparison of total kink energies in (a) and (b) states shows which state (a or b) is more stable. We consider the state that has the lower kink energy level as the more suitable one (Fig. 4(a and b)).

This method is similar for all cells and their values, because of lack of space, first part of proof stated and the rest of relations omitted.

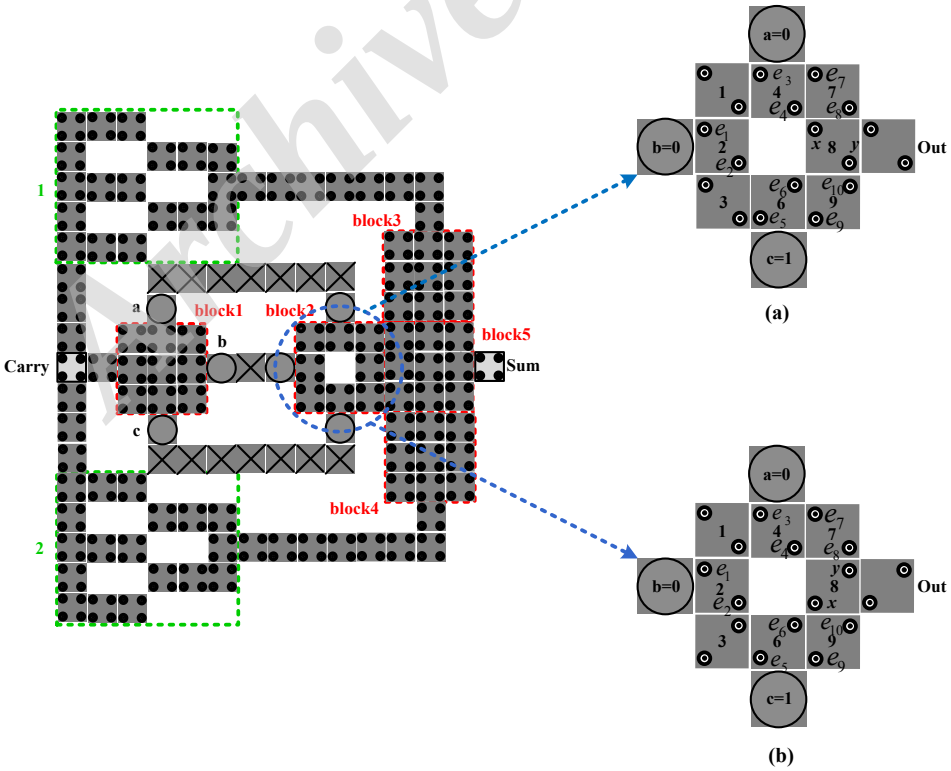

Fig. 4: (a) The zero value in cell 8 (b) The one value in cell 8.

Fig. 4(a) (electron x)

$$U_1 = \frac{A}{r_1} = \frac{23.04*10^{-29}}{26.9*10^{-9}} \approx 0.86 * 10^{-20}\ (J)$$

$$U_2 = \frac{A}{r_2} = \frac{23.04*10^{-29}}{38*10^{-9}} \approx 0.61 * 10^{-20}$$

$$U_3 = \frac{A}{r_3} = \frac{23.04*10^{-29}}{18.1*10^{-9}} \approx 0.61 * 10^{-20}\ (J)$$

$$U_4 = \frac{A}{r_4} = \frac{23.04*10^{-29}}{120*10^{-9}} \approx 1.15 * 10^{-20}\ (J)$$

$$U_5 = \frac{A}{r_5} = \frac{23.04*10^{-29}}{20.1*10^{-9}} \approx 1.15 * 10^{-20}\ (J)$$

$$U_6 = \frac{A}{r_6} = \frac{23.04*10^{-29}}{42.9*10^{-9}} \approx 0.54 * 10^{-20}\ (J)$$

$$U_7 = \frac{A}{r_7} = \frac{23.04*10^{-29}}{2.83*10^{-9}} \approx 8.14 * 10^{-20}\ (J)$$

$$U_8 = \frac{A}{r_8} = \frac{23.04*10^{-29}}{28.3*10^{-9}} \approx 0.81 * 10^{-20}\ (J)$$

$$U_9 = \frac{A}{r_9} = \frac{23.04*10^{-29}}{28.4*10^{-9}} \approx 0.81 * 10^{-20}\ (J)$$

$$U_{10} = \frac{A}{r_{10}} = \frac{23.04*10^{-29}}{4*010^{-9}} \approx 0.58 * 10^{-20}\ (J)$$

$$U_{T_{11}} = \sum_{i=1}^{10} U_i \approx 15.9 * 10^{-20}(J)$$

$$U_{T_1} = \sum_{i=1}^{2} U_{1i} \approx 36.3 * 10^{-20}(J)$$

Fig. 4(a) (electron y)

$$U_1 = \frac{A}{r_1} = \frac{23.04*10^{-29}}{2*10^{-9}} \approx 11.52 * 10^{-20}\ (J)$$

$$U_2 = \frac{A}{r_2} = \frac{23.04*10^{-29}}{26.9*10^{-9}} \approx 0.86 * 10^{-20}\ (J)$$

$$U_3 = \frac{A}{r_3} = \frac{23.04*10^{-29}}{20*10^{-9}} \approx 1.15 * 10^{-20}\ (J)$$

$$U_4 = \frac{A}{r_4} = \frac{23.04*10^{-29}}{42.05*10^{-9}} \approx 0.55 * 10^{-20}\ (J)$$

$$U_5 = \frac{A}{r_5} = \frac{23.04*10^{-29}}{6.63*10^{-9}} \approx 3.48 * 10^{-20}\ (J)$$

$$U_6 = \frac{A}{r_6} = \frac{23.04*10^{-29}}{42.9*10^{-9}} \approx 0.54 * 10^{-20}\ (J)$$

$$U_7 = \frac{A}{r_7} = \frac{23.04*10^{-29}}{28.3*10^{-9}} \approx 0.81 * 10^{-20}\ (J)$$

$$U_8 = \frac{A}{r_8} = \frac{23.04*10^{-29}}{53.7*10^{-9}} \approx 0.43 * 10^{-20}\ (J)$$

$$U_9 = \frac{A}{r_9} = \frac{23.04*10^{-29}}{40*10^{-9}} \approx 0.58 * 10^{-20}\ (J)$$

$$U_{10} = \frac{A}{r_{10}} = \frac{23.04*10^{-29}}{43.9*10^{-9}} \approx 0.52 * 10^{-20}\ (J)$$

$$U_{T_{12}} = \sum_{i=1}^{10} U_i \approx 20.4 * 10^{-20}(J)$$

Since cells 1 and 3 are roughly in a long distance from cell 8, their potential energy can neglect. Please note the value of cell 8 transferred to the output cell, which give us a majority decision of inputs a, b and c.

Fig. 4 (b) (electron x)

$$U_{T_{21}} = \sum_{i=1}^{10} U_i \approx 18.1 * 10^{-20}(J)$$

$$U_{T_2} = \sum_{i=1}^{2} U_{2i} \approx 40 * 10^{-20}(J)$$

Fig. 4(b) (electron y)

$$U_{T_{22}} = \sum_{i=1}^{10} U_i \approx 21.9 * 10^{-20}(J)$$

Comparison achieved results, electrons in cell 8 positioned in states (a) with more stability and lower potential energy. It is worth mentioning that in all cells U_{T1} is the potential energy in +1 polarization and U_{T2} is the potential energy in -1 polarization.

By considering middle cells in block2 (Fig. 3) the results summarize in Table 1.

The following observation can made from Table 1:

1. A proposed scheme with single defective cell function as MV/MV like.

2. Defective cell occurring corner cells (cells 1, 3, 7 and 9) does not change the logic function of block2, thus confirming the none-defect tolerant design of a single-bit full-adder.

3. Whenever cell 8 is defective, the polarization level experiences a drop (about ±0.1), but it also acts as majority gate.

4. Schemes block1, block2, block3, block4 and block5 similar one another and schemes 1 and 2, significant specifications of proposed design is tolerating multi-faults. For instance, if one of the mentioned faults in “Faults and Fault tolerance” section simultaneously occurs in block1, block2 and block 3 or 1 and 2 schemes, the proposed structure will still perform proper; that can prove by physical relations.

Considering computing, we can infer the proposed structure for implementing a fault-tolerant full-adder is correct and resulted in a correct state for the output cell when faults occur.

Power dissipation analysis

Based on the small size of QCA designs, power is another important design parameter [24]. Here, we consider upper bounds of switching and leakage power that will occur with different input vectors.

The power dissipated at each cell is the function of the rate of change of the clock energy (γ). E_k is referred the kink energy that stated in pervious section; and energy dissipated over a specified time period can be arrived at by integrating power dissipation [24].

Table 2 shows the results of energy dissipated in proposed design. As we can see from the table, it has 126 energy dissipating QCA cells present in its layout.

Simulation results

For the proposed circuit layout and functionality checking, a simulation tool for QCA circuits, QCADesigner version 2.0.3 [45], is used. QCADesigner gives the designer the ability to quickly layout a QCA design by providing an extensive set of CAD tools. As well, several simulation engines facilitate rapid and accurate simulation. This tool has already been used to design full-adders, barrel shifters, random-access memories, etc. These verified layouts provide motivation to continue efforts toward a final implementation of QCA circuits [46]. The following parameters are used for bistable approximation that is adequate for simulations of basic circuits: cell size=18 nm, number of samples=50000, convergence tolerance=0.0000100, radius of effect=65.000000 nm, relative permittivity=12.900000, clock high=9.800000e-022 J, clock low=3.800000e-023 J, clock shift=0, clock amplitude factor=2.000000, layer separation=11.500000 and maximum iterations per sample=100. Most of the mentioned parameters are default values in QCADesigner.

Figs. 5 and 6, show layout and simulation results of proposed design.Layout of previous designs and their simulation results are prepared and compared in this section. Simulation results reveal the proposed design is more robust than the previous designs. Table 3 explained the differences among the traditional QCA design with presented designs.

Table 1: Single defective cell in proposed scheme.

Defective Cell No.	Out	Defective Cell No.	Out
None	M(a,b,c)	1	M(a,b,c)
2	M(a,b,c)	3	M(a,b,c)
4	M(a,b′,c)	5	M(a,b,c)
6	M(a,b,c′)	7	M(a,b,c)
8	M(a,b′,c′)	9	M(a,b,c)

Table 2: Energy dissipated in proposed design.

γ/E_k	0.5	1.0	1.5
Avg E_d	340.06	402.56	587.24
Max E_d	592.91	699.78	735.65
Min E_d	89.34	198.23	376.55

Table 3: Comparison of QCA full-adders.

	Cell count	Delay	Avg E_d (1.0)	Fault tolerance
Previous design [1]	192	Not applicable	640.67	No
Previous design [8]	322	3 clock phases	1160.69	Yes
Previous design [9]	138	3 clock phases	587.34	Yes
Proposed design	126	3 clock phases	402.56	Yes

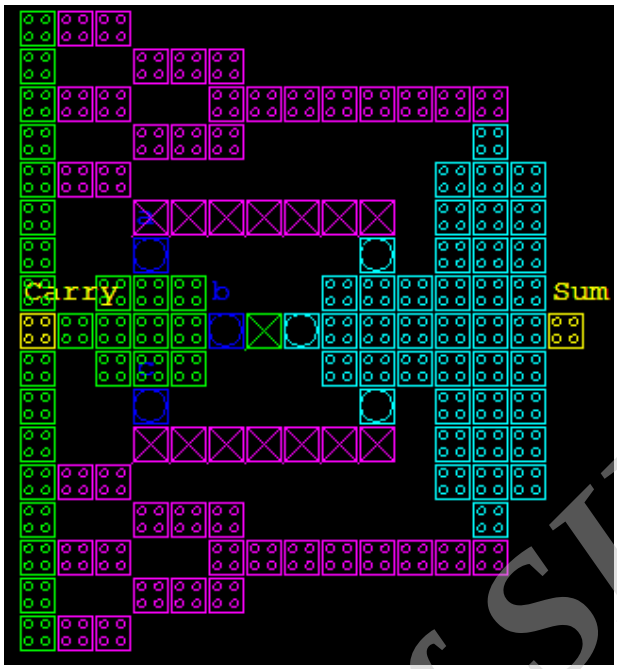

Fig. 5: Layout of proposed fault-tolerant full-adder.

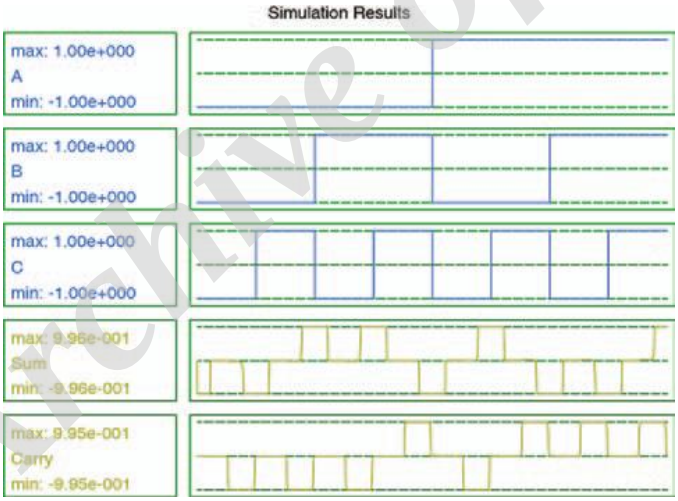

Fig. 6: Simulation results for proposed fault-tolerant full-adder.

CONCLUSION

A novel expandable fault-tolerant full-adder cell for quantum-dot cellular automata is presented first in this paper. High performance logic component can achieve by using this fault-tolerant full-adder. Some physical proofs and computer simulations have verified the functionality of the presented structure. Also power dissipation analysis shows that the presented circuit will be useful to circuit designers in providing a more complete view of the QCA operations. The proposed design proves significantly more robust than the standard full-adder to single or multi-faults in misalignment cells, missing cells and dislocation cells.

CONFLICT OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this manuscript.

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