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REVIEW ARTICLE

A study of emerging semi-conductor devices for memory applications

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Abstract

In this paper, a study of the existing SRAM (Static Random Access Memory) cell topologies using various FET (Field Effect Transistor) low power devices has been done. Various low power based SRAM cells have been reviewed on the basis of different topologies, technology nodes, and techniques implemented. The analysis of MOSFET(Metal Oxide Semiconductor Field Effect Transistor), FinFET(Fin Field Effect Transistor), CNTFET (Carbon Nano Tube Field Effect Transistor), and TFET (Tunnel Field Effect Transistor) based SRAM cells on the basis of parameters such as stability, leakage current, power dissipation, read/write noise margin, access time has been done. HSPICE, TCAD, Synopsys Taurus, and Cadence Virtuoso were some of the software used for simulation. The simulations were done from a few μms to 7nm technology nodes by different authors.

Keywords: *CNTFET; FinFET; Leakage Current; MOSFET; SRAM; TCAD; TFET.*

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INTRODUCTION

MOSFET is one device that has been used in the IC (Integrated Circuit) industry since many decades and it has survived the test of the time. Most of the modern day application circuits that we use today have been driven by CMOS (Complementary Metal Oxide Semiconductor) technology which makes use of both NMOS (N-Channel Metal Oxide Semiconductor) and PMOS (P-Channel Metal Oxide Semiconductor) devices. A MOSFET device can easily work as a switch, and this property of MOSFET is generally used in digital logic circuits and memories. As we approach Deep Sub-Micron (DSM) and Ultra Deep Sub- Micron (UDSM) technologies; MOSFETs when scaled down to that level, results in reduced power consumption, cost effective production and better device performance. But at the same time, smaller devices lead to various Short Channel Effects (SCEs) which impact the working of the device adversely. Various innovations have been done at the device level to overcome the short channel effects that arise in the MOSFET device because of scaling. Static power component is getting comparable to active or dynamic power of any MOSFET based circuits, with the rigorous scaling in dimensions of the MOSFET device.

Gorden Moore in the year 1965 estimated (Fig. 1) the exponential growth of number of transistors in integrated circuits. These days, there are billions of transistors found in an IC [1]. As per the roadmap proposed by ITRS (International Transactions Reporting System) [3], it is expected that planar devices would not prove to be

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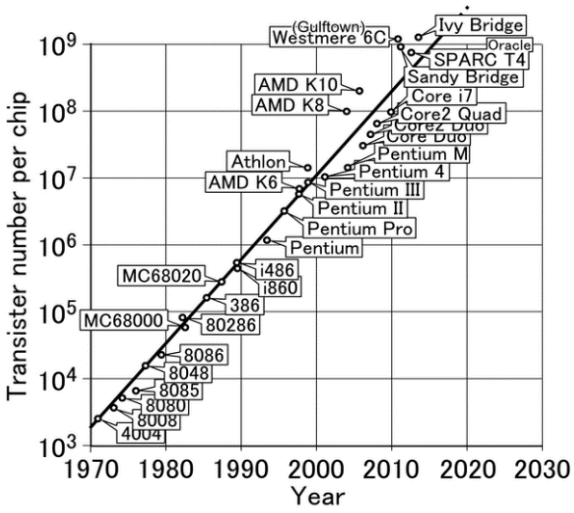

Fig. 1. Transistor count as a function of year as per Moore's Law [2].

effective from leakage point of view when the device dimensions go below 32nm. Scaling has led to various advantages like enhancement in the transistor device density and improvement in the performance of IC. The overall device performance improves but there is always a trade-off between the device performance metrics like on current, off current and Sub threshold Swing (SS) [4–6].

In a MOSFET device, due to channel shortening, the gate control over the channel electrostatic properties becomes weaker and potential at the drain end impacts the channel electrostatic properties significantly. This leads to the fact that gate will not be able to control the device operation and this further leads to enhancement in the off current which thereby worsens the device performance. High-k dielectric materials and thinner gate oxides can be used to palliate the issue by further elevating the capacitance that exists between channel and region. At the device level, it is difficult to reduce the oxide thickness below a particular value because doing that leads to increase in the leakage current induced by the gate, also popularly known as GIDL (Gate Induced Drain Leakage) [7–9]. One of the strategies that are used to combat this issue is to deploy Multiple Gates (MG) instead of single gate. MGs provide better control of channel electrostatic properties thereby leading to better device performance in terms of low leakage [10–15]. So MGFETs referred to as FinFETs are emerging as better alternative to planar MOSFETs in terms of short channel performance metrics, like Threshold voltage (V_{th}) roll off, Drain-Induced Barrier Lowering (DIBL) and sub threshold slope. Other alternative devices are CNTFETs and TFETs. CNTFET devices offer increased channel mobility and improved gate capacitance. While TFET offers steep sub threshold slope.

The paper is organised as follows: In section 2, CMOS (Complementary Metal Oxide Semiconductor) based SRAM has been discussed briefly. In section 3, most popular low power devices have been discussed along with their latest techniques and circuit topologies for SRAM applications. In Section 4, review of various works done on SRAM based on MOSFET, FinFET, CNTFET and TFET has been presented in tabular form. Conclusion of the work is drawn in section 5.

SEMICONDUCTOR MEMORY: SRAM

Semiconductor memory is the integral part of any digital system. Nowadays, the use of memory has boomed because of the requirement of large amount of storage. To address this growing need of semiconductor memories, various technologies and types are employed. Thereby new technologies are taking birth and the existing ones are being further developed. According to the specific application, variety of memory types is available and one of them is SRAM (Static Random Access Memory).

SRAM is volatile in nature. In it, two inverters are connected back to back. To store data at a specific memory location, one row and one column are selected with the help of a decoder/driver. The intersection point of the selected row and column

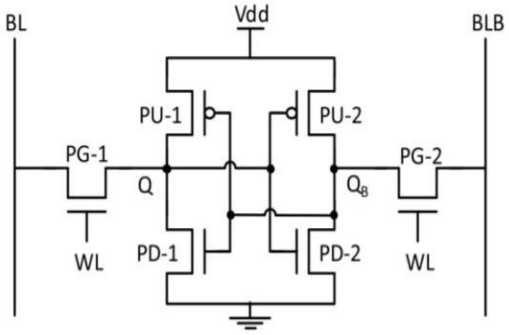

Fig. 2. Conventional Six Transistor SRAM Cell [16].

is known as memory cell. The output is sensed by the sense amplifier and the output buffer gives the output. The access time of each memory cell is same (irrespective of the memory location); hence they are known as Random Access Memory. SRAM exists as Bipolar SRAM, MOS SRAM, CMOS SRAM and Bipolar CMOS SRAM. CMOS based SRAM has been discussed in this section briefly.

CMOS SRAM

The schematic of a six transistor based SRAM cell is given in the Fig. 2, in which PU, PD and PG are Pull Up transistors, Pull Down transistors and Pass Gate transistors respectively. It has two cross coupled inverters (PU-1: PD-1 and PU-2: PD-2) forming a latch. The latch is used for data retention. Two pass gate transistors (PG-1 and PG-2) are connected to Bit Lines (BL and BLB) [16]. In short, the operation of SRAM includes the selection of particular row and column from the SRAM array. When a particular column is selected, the cell connected to the associated Word Line (WL) goes high. When a particular row is selected, the cell is connected to the bit lines (BL and BLB) respectively. Depending on the state of individual transistor of the cell, the BL and BLB voltages are going to change [17].

The BL and BLB voltages are kept at a pre-charged value and are equated initially. When one BL goes up the pre-charged value by small amount and then the other BL goes down by a small amount. Hence when some difference is created in the voltages due to the state of the cell then the sense amplifier is turned on. One of the bit lines goes high and other goes low, thus selecting one cell in the column (This is done for all the columns). As the pass gate transistors are present above the decoder, the decoder selects only one of the columns which are connected to the input/output line. The information present on that particular column is passed on to the input/output (I/O) lines.

Read Operation

In it, BL and BLB are pre-charged to the supply voltage and WL is set, due to which PG-1 and PG-2 are enabled. The stored values present at Q and Q_B are forwarded to the BL and BLB, resulting in the discharging of BL through PG-1 and PD-2, thus leaving the BLB at it pre-charged value. Afterwards the value at Q is read.

Write Operation

These I/O lines are used to write information into the cell by forcing the voltages on the bit lines. When one of the bit lines is made high and other is made low then a bit can be written into the particular cell [17]. In write mode of operation, PG-1 transistor resists PU-1 in order to discharge node voltage at Q. In write operation, BLB and WL are set.

Hold Operation

In hold mode of operation, WL is disabled. Hence the access transistors (PG-1 and PG-2) are turned off. The BL and BLB are disconnected from the latch and the entire data is held in the latch.

LOW POWER DEVICES : TECHNIQUES AND TOPOLOGIES

There are four most commonly used transistors for designing SRAMs namely MOSFET, FINFETs, TFETs and CNTFETs. The comprehensive and circuitry review of these devices in respect of SRAM domain has been summarized in this work.

MOSFET Based SRAM Cells

The building blocks of VLSI chips are silicon MOSFETs [18]. Also known as the Insulated Gate FET. The cross sectional view of conventional NMOS MOSFET is shown in Fig. 3.

It is a NMOSFET in which a lightly doped P substrate is diffused with heavily doped N type regions acting as Source (S) and Drain (D). Region between source and drain acts as channel with channel length L. The operation of the MOSFET is controlled by the gate voltage which may be either positive or negative (depending on the depletion or enhancement type of MOSFET) as the gate is insulated from the channel using oxide.

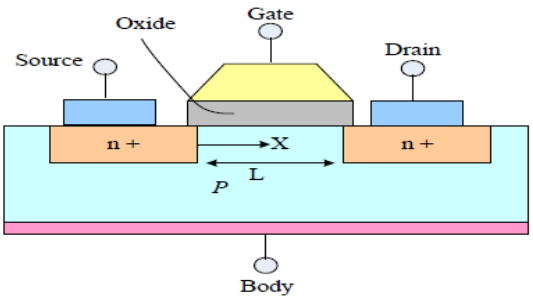

Fig. 3. Conventional MOSFET [19].

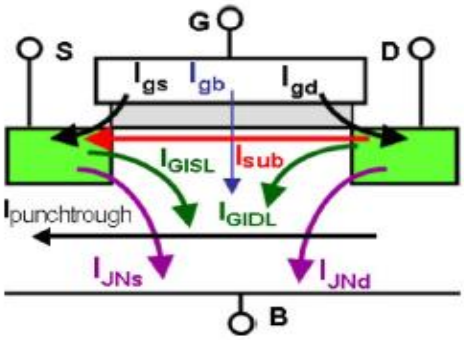

Fig. 4. Leakage current components in MOS [20].

To improve the package density while keeping the fabrication cost low, various efforts are being made to scale the dimensions of the transistor. To control the short channel effects, which come into picture when the device is scaled down; gate oxide thickness is required to be scaled down. This leads to the high tunneling current into the gate insulator of the transistor [21].

Leakage mechanisms are majorly of three types (shown in Fig. 4): Gate oxide leakage currents from gate to source (I_{gs}), gate to bulk (I_{gb}) and gate to drain (I_{gd}), Sub-threshold leakage current (I_{sub}) and Reverse Bias PN Junction leakage (I_{JNs} and I_{JNd}). The other leakage components that could be neglected when the device operates in normal mode are punch through current and GIDL [5].

A half select disturb free 11T SRAM Cell is introduced for ultra low voltage operations by Yajuan He, et.al in ref. [22]. The introduced SPG11T (Shared Pass Gate) SRAM is compared with 6T, 8T[23], BI10T [24], 9T[25], PNN10T [26] and 11T [27] SRAM at 40nm CMOS technology node using 0.5V supply voltage. The comparison is done based on HSPICE simulations in terms of RSNM (Read Static Noise Margin), WM (Write Margin), leakage power and area. This design is developed to enhance the soft error immunity. To achieve significant power reduction, a column selection enabled 10T SRAM is introduced in ref. [28]. To improve the write ability, the differential VDD technique is used. The simulations are carried out for 65nm CMOS technology node. The proposed 10T SRAM exhibits reduction in leakage power when compared with existing single ended 10T SRAM.

To improve the read access speed and write margin in advanced technology nodes of CMOS; buried powered SRAM is introduced in ref. [16]. The simulations are carried out for the netlist extracted in Cadence assuming 3nm CMOS technology. This proposed buried powered SRAM is best for high performance, high density and low power memory systems in advanced processors. 6T CMOS SRAM at 65nm technology node having minimum size transistors is proposed in ref. [29]. The advantages of this design are cost reduction, less leakage currents and lower dynamic energy requirements. The most affected parameter of the design is read stability. However, this effect can be overcomed by the read assist circuits.

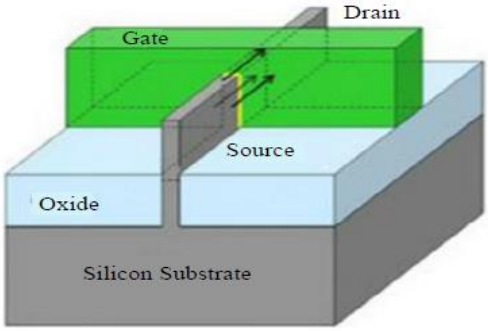

Fig. 5. 3D FinFET Structure [39].

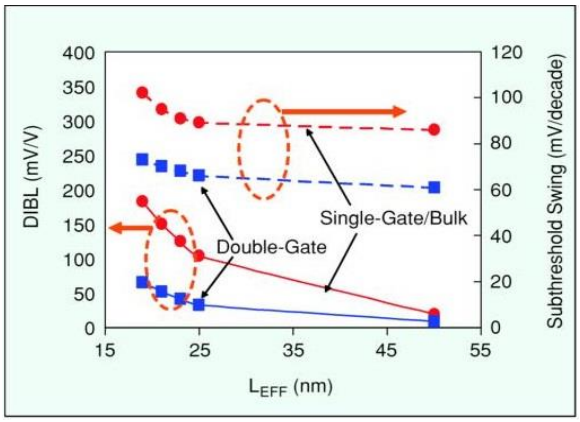

Fig. 6. DIBL and Subthreshold Swing (SS) versus effective channel length [15].

In the work by Anuj Grover, et.al [30], SRAM cell co-designed with layout and assist schemes is introduced for the operation of SRAM in Wide Voltage Range (WVR) from 0.35 to 1.2V. The 32KB SRAM cell is fabricated in 28nm UTBB-FDSOI (Ultra Thin Body and Buried Oxide-Fully Depleted Silicon on Insulator) technology for benchmarking various implementations of WVR and low voltage SRAM. Figure of Merit is also proposed, which may help the designers to optimally choose the design and to improve energy efficiency. An 8T 32 KB SRAM cell design is proposed in ref. [31]. The simulations are performed in 90nm CMOS technology for the proposed 8T cell and the conventional 6T SRAM cell. During write operation, this 8T SRAM cell along with feedback interrupt improves the write ability. It can also operate at small supply voltage 0.43V. Internal write back scheme is also presented to remove the half selection problem.

FINFET Based SRAM Cells

MG (Multi Gate) MOSFETs are considered as an alternative of planar MOSFETs. In Double Gate MOSFETs (DGFET), as compared to the conventional gate, a second gate is added to provide good control over SCEs. In it, both gates switch simultaneously. In DGFET, the drain produced longitudinal EF (Electric Field) is blocked from source end of the channel, because of which DIBL is reduced and sub threshold swing improves. Fabrication of self aligned DG has been challenging in DGFETs. So in order to address this issue, fin type double or triple gate MOSFETs were studied in 1989. This was the time when double gate SOI structure was fabricated by Hisamato et.al [32], which they called DELTA (DEpleted Lean channel TrAnsistor). Due to degrading Short Channel behaviour of MOSFETs, FinFETs are gaining attention over the past decade [33-38].

Fig. 5 shows the tri-gate FinFET structure proposed by Intel. FinFET is a multi gate FET in which gate is wrapped around the conducting channel called Fin. In Fig. 6, Short Channel performance of planar MOSFETs is compared with that of DG FinFETs having same channel length.

Alexandra et.al [40] explains the impact of

PVT (Process, Voltage, Temperature) Variations on power consumption and performance for different transistor sizing techniques in FinFET technologies. Results are calculated for 14nm FinFET technology. This paper defines the contributions of the variability in design steps and in selection of the most suitable transistor sizing technique for specific applications.

Techniques for dynamic supply boosting are described to enable very low voltage operations. The work in [41] focusses on 8T SOI FinFET SRAM for 14nm technology. For the on demand boosting of power supply, two concepts have been explained. In first technique, a capacitive coupling of interconnects and FinFET device is employed to boost Vdd [42]. In the second novel technique, an inductor is added to the boosting structure. This novel technique provides improved access time, V_{min} and power consumption. In ref. [43], 128 MB 6T SRAM for 10nm FinFET is used for exploring the different SRAM assists to have the best power, performance and area (PPA) gain. High density 6T 0.040 um^2 and high power 6T 0.049 um^2 bit cells are demonstrated for analysing PPA with assist.

While working with advanced technologies like 22nm FinFET in average 8T SRAM, there are large variations in threshold voltage. Thus, the boosted word line voltage cannot be used, as this will degrade the read stability of SRAM and also increases the read delay. In ref. [44], differential SRAM architecture is proposed having a full swing local Bit line. The proposed 22nm FinFET SRAM cell offers small read delay with lesser area compared to average 8T SRAM. This proposed SRAM architecture is energy efficient.

An ultra low voltage one-port 12T SRAM compiler is designed at 7nm FinFET technology [45]. This design attains the lowest V_{min} of 290 mv reported so far. It is noted that better energy saving is achieved even at lower voltages in the proposed design in comparison to six transistor based dual rail compiler. This is because the voltage scaling of 6T SRAM compiler is constrained by the V_{min} of 6T SRAM. Various features are supported by the compiler design such as column multiplexing, BW (Bit Write) functionality, PM (Power Management) and test features. This design offers minimum area overhead.

It is known that power gating is used for leakage current reduction in SRAMs. In ref. [46], three techniques have been evaluated for reduction in leakage power and EDP (Energy Delay Product), of 6 transistor and 8 transistor FinFET SRAM cells. The techniques used are: Power Gating technique, Near Threshold operation at VDD 0.6V and SRAM cells with Short Gated (SG) and Low Power (LP) configured FinFETs. This analysis shows that power gating is beneficial for the SRAM cells having higher leakage since power gating provides the largest reduction in leakage current. Near threshold operation is used for the SRAM cells with low leakage to further reduce the leakage current. These design techniques would enable longer battery life for sensor systems and higher reliability for IoT applications. In ref. [47], TCAD simulations are carried out to examine the Self Heating Effect (SHE) in 14nm SOI FinFET and bulk FinFET. The calibration is also performed for I_D-V_G curve based on the experimental data released by Intel in 2014 [48] for bulk FinFET and by IBM [49] for SOI FinFET. In bulk FinFET, the heat diffuses vertically towards the substrate and then to the heat sink. In Silicon on Insulator FinFET, heat is dissipated to source, drain and gate followed by the heat sink. Various optimizations are proposed for SHEs.

The implementation of Gain-Cell embedded DRAM (GC-eDRAM) is discussed for the first time by Robert Giterman, et. Al [50]. This design offers two times higher bit cell density in respect to 6T SRAM in 16nm FinFET technology. This is the good option for operating cells at low voltage because in GC-eDRAM, the leakage could be controlled for high temperatures. The Data Retention Time (DRT) is also improved. For the circuit to consume minimum energy, it should operate near V_{th} region. This concept is employed by Keonhee Cho et.al in [51]. They proposed 9T SRAM cell with one sided Schmitt Trigger inverter based on 22nm FinFET technology. A comparative analysis is done with some existing SRAM topologies in terms of energy and area. Also the proposed design offers low energy consumption and improved write ability, hold stability and read stability yields without employing write back scheme in bit interleaving structures. To evaluate the impact of device design parameters on circuit level, a quantum physical device circuit co-design is introduced using 6T SRAM cell in 7nm FinFET technology. A 1:2:1 SRAM cell is proposed in [52] because it provides appreciable balance between static power dissipation, delay and stability even under process fluctuation. This design achieves leakage reduction, and improvement in Hold Noise Margin (HNM) and Write Margin (WM). Delay comes out to be the design trade off. This work provides direction for the researches on 5nm node and beyond.

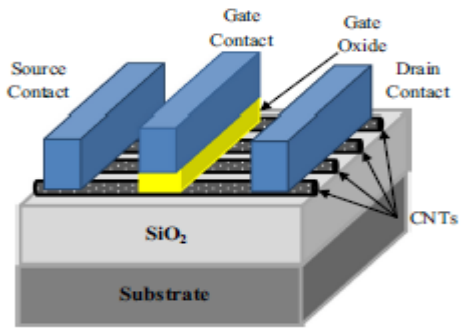

Fig. 7. CNTFET Device Structure [54].

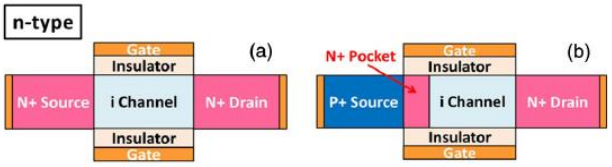

Fig. 8. a) n type MOSFET Structure b) n type p-n-p-n TFET Structure [59].

Carbon Nano Tube Field Effect Transistor (CNTFET) Based SRAM Cells

Carbon Nano Tube Field Effect Transistor based devices are getting much importance as they offer increased channel mobility and improved gate capacitance. CNTFET employs CNT as their semiconducting channels. Graphene can roll up and form a hollow cylinder called CNT [53]. The 3D CNTFET structure is given in Fig. 7 [54].

Single Walled CNT (SWCNT) consists of one cylinder only, having diameter close to 1 nm. On the basis of angle of the atomic arrangement along the tube, a SWCNT can be either a conductor or a semiconductor. This is defined by the chirality vector which is given by the integer pair (n, m). If n = m or n-m = 3i then CNT behaves as metallic; where i is an integer, otherwise it is semiconducting in nature [55]. The diameter of CNT is calculated using Equation 1 [53].

$$D_{CNT} = \frac{\sqrt{3}a^{\circ}}{\pi}\sqrt{n^2 + m^2 + mn} \quad (1)$$

Where a_o is inter atomic distance between two carbon atom neighbors (a_o= 0.142 nm). In ref. [53], the effect of oxide thickness variation on gate capacitance is analysed for single and double gate MOSFET, CNTFET and silicon nanowire FET devices. Extensive simulations are carried out using the nanoHUB tools [56]. It is evident that performance is degraded in single and double gate MOSFETs whereas silicon nanowire FET and CNTFET devices offer improved threshold voltage and propagation delay and less leakage in deep nanometer nodes. CNTFET is advantageous in terms of power consumption and noise immunity compared to conventional CMOS SRAMs. Fabrication process of non ideal CNT generates semiconductor-CNTs (s-CNTs)and metallic CNTs (m-CNTs). Due to this, faulty cells are generated along m-CNTs growth's direction. Hence a test is required to detect these faults. In ref. [57], a low cost test is proposed which achieves high fault coverage by employing three jump test algorithm. Furthermore, m-CNT generated SRAM faults are modelled. Their distribution in SRAM array is characterised.

Performance of CNTFET is varied due to spatial distribution of Carbon Nano Tube (CNT). This impact is studied in [58], by performing monte carlo simulation. Approximately 10% lower current is observed in spatial distribution of CNT to that of uniform distribution. The SRAM SRNM (Static Read Noise Margin) is also evaluated by this approach.

Tunnel Field Effect Transistor (TFET) Based SRAM Cells

TFET offers steep subthreshold slope and becomes a promising candidate for ultra low voltage operation as compared to conventional MOSFETs. Structures of n type MOSFET and n type p-n-p-n TFET [59] are shown in Fig 8(a) and Fig 8(b) respectively. A detailed analysis of TFET is performed in ref. [60]. Also the performance/ stability of various TFET SRAM cells has been analysed by using TCAD mixed mode simulations. A 7T Driver Less (DL) TFET SRAM cell is proposed having improved hold, write, and read stability and performance.

In ref. [61], a study of implementing TFET structures calibrated against state of art devices and idealised template TFETs [62,63] is presented using TCAD mixed mode simulations. In order to address the unidirectional current limit of TFET when employed in 6T SRAM, TFET templates having better characteristics are used. Device to device variation, is the key challenge for scaling beyond 10nm technology nodes.

In ref. [64], a comprehensive study of Side Wall Roughness (SWR) and variation effects in TFET and FinFET has been presented. 3D-TCAD numerical simulations have been carried out for the devices GaSb-InAs n/p-HTFETs, Si bulk n/p-FinFETs, Ge

bulk p-FinFETs and $In_{0.53}Ga_{0.47}As$ bulk n-FinFETs. Furthermore, 6T SRAM cell configuration with FinFETs and 10T SRAM configuration with HTFETs (Hetrojunction TFETs) are studied at 22nm technology node.

REVIEW OF WORK DONE BY AUTHORS ON LOW POWER DEVICES

In this section, a review of the work done by various authors on the above low power devices is given in Table 1,Table 2, Table 3, Table 4 and Table

Table 1. Review summary of various CMOS based SRAM cell designs.

Ref.	Device/ Technology	Software Used	Technique	Parameters Worked on by the Authors	Remarks
[22]	CMOS/ 40nm	HSPICE	11T SRAM	Leakage Power, Area, RSNM & Write margin	SPG 11T (Shared Pass Gate) SRAM is designed to enhance soft error immunity.
[28]	CMOS/ 65nm	Not Mentioned	10T SRAM	Dynamic power, Leakage power & Short cut power	In order to improve the write ability of the proposed design, the differential VDD technique is adopted.
[29]		Not Mentioned	6T SRAM	Write ability, Read ability, Read time, Power consumption, Cell Area & Leakage current	Read stability is affected most by decreasing the cell ratio.
[30]	CMOS/ 28nm	Not Mentioned	8T 32 KB SRAM	Power delay product & Figure of merit	For achieving wide voltage range operation, an optimized co design of SRAM, its layout & assist schemes are proposed.
[31]	CMOS/ 90nm	Not Mentioned	8T 32 KB SRAM	Power consumption, Delay, Read SNM Write ability	Internal write back scheme is presented to remove the half select problem
[65]	CMOS/ 90nm	Not Mentioned	9T SRAM	Read & write stability (Cell performance)	To achieve the deep subthreshold operation & to improve the write margin, DAFC (Data Aware F/b Cutoff) scheme is used.
[66]		Cadence Virtuoso	10T SRAM	Write time, Write margin	TGA (Transmission Gate Access) 10T SRAM with write assist technique is compared with 8T SRAM with and without write assist technique.
[67]	CMOS/ 65nm	Hybrid Simulator	6T and 4T cells composed of transistors having Dynamic Double Gate structure	Area, Speed, Standby Power	Yin-Yang Feedback Technique (Back Gate Bias Technique)
[68]		Not Mentioned	11T SRAM	Write & Read Power, Standby Leakage Power, Read stability, Write Trip Voltage, Write Trip Current, Area	Low Stress SRAM cell called IP3 SRAM Bit Cell (11T) with drowsy supply voltage when the cell is in standby.
[69]	CMOS/ 45nm	HSPICE	6T SRAM	Gate Leakage, Static Power Dissipation, Read/Write performance, Stability, Area	6T SRAM with low gate leakage technique: 1. Improved write line voltage control. 2. PMOS Pass Transistor
[70]	CMOS/ 40nm	Cadence	5T SRAM	Static power reduction	Sub Threshold (ST) 5T SRAM
[71]	CMOS/ 22nm	HSPICE	11T SRAM	FOM, Read Stability, Write ability, Hold SNM, Read & Write access time and power, Leakage power, SAPR ratio	11T ST Based Single Ended SRAM (Feedback Mechanism of ST)
[72]	MOSFET/ 20nm	TCAD	GAA SiNS MOSFET	Drive current, On/Off ratio & device yield	GAA SiNS MOSFET is a promising candidate for area scaling & improved power performance.

Table 2. Review summary of various FinFET based SRAM cell designs.

Ref.	Device/ Technology	Software Used	Technique	Parameters Worked on by the Authors	Remarks
[40]	FinFET/ 14nm	HSPICE	Different transistor sizing technique	Process, Voltage & Temperature variations, Power Delay Product	This paper defines the contributions of the variability in design steps & in selection of the most suitable transistor sizing technique for specific applications.
[41]		Not Mentioned	8T SOI SRAM	Power consumption & access time	Dynamic supply boosting techniques are described.
[43]	FinFET/ 10nm	Not Mentioned	128 Mb 6T SRAM	PPA (Power, Performance & Area)	High density 6T 0.040 μm^2 & high power 6T 0.049 μm^2 bit cells are demonstrated for analyzing PPA with assist.
[44]	FinFET/ 22nm	HSPICE	Differential SRAM architecture v/s average 8T SRAM	Read stability, Read delay, Area & Energy	Energy efficient SRAM architecture is proposed.
[45]	FinFET/ 7nm	Not Mentioned	12T SRAM compiler	Area, Energy consumption & Leakage	Various features are supported by the compiler design such as column multiplexing, Bit Write functionality, Power Management & Test features.
[46]	FinFET/ Not Mentioned	Synopsys MEDICI	6T & 8T SRAM	Leakage power, Energy Delay Product, SNM	Power Gating is beneficial for SRAM cells having higher leakage & Near threshold operation is used for the SRAM cells with low leakage.
[47]	FinFET/ 14nm	TCAD	Bulk & SOI FinFET	I_{OFF}, DIBL & SS	Impact of fin size, BOX, Doping concentration, Thermal conductivity & ambient temperature on SHE (Self Heating Effect) is studied.
[51]	FinFET/ 22nm	HSPICE	9T SRAM	Energy, Area, Write ability, Hold stability & Read stability, DIBL, SS & Leakage power	For circuit to consume minimum energy, it should operate near V_{th} region.
[52]	FinFET/ 7nm	TCAD	6T SRAM	Delay, Stability, Power dissipation, Leakage, HNM, RNM, WM & Area	The proposed design provides appreciable balance between static power dissipation, delay & stability even under process fluctuations.
[73]	FINFET/ 1µm	TCAD	(GAA NS-JLFET) with trench and raised source and drain structure.	On/Off current, DIBL, Subthreshold slope	The proposed design exhibits good electrical properties with higher mobility, steep subthreshold slope, lowered DIBL & high On/Off current ratio.
[74]	FINFET/ 0.11µm	TCAD	IDG-FinFET (Independent Double Gate FinFET)	Leakage current and dynamic power consumption	Reduced leakage current and power consumption by controlling Vth of IDG-FinFET
[75]	FINFET/ 45nm	Taurus Devices Simulator	6T SRAM	Leakage power, SRAM stability, Access Time, Write time analysis, Read Failure analysis, Cell area	Under process variation, improved stability with less leakage power.

Continued Table 2. Review summary of various FinFET based SRAM cell designs.

Ref.	Device/ Technology	Software Used	Technique	Parameters Worked on by the Authors	Remarks
[76]	FINFET/ 30nm	TCAD	3D DG-FinFET	I_{ON}, I_{OFF},V_{th}	It provides low leakage and improved drive current. Also meets the requirement for Low Power Multi Gate technology predicted by ITRS 2013.
[77]		TCAD	3D MuGFETs	I_{ON}, I_{OFF},$V_{th,}$ Delay, Trans conductance, SS	Drive current and trans conductance of the device linearly increases with increase in fin height
[78]		TCAD		Feasibility of 3D process simulation flow in context of optimization of device & fabrication processes	This paper targets to show feasibility of the flow of 3D process simulation in regard to device design optimization and underlying fabrication processes.
[79]	FINFET/ 30/25/20n m	TCAD	Analysis of impact of various random variations on device performance	Relation b/w I_{ON}, I_{OFF},V_{th}, SS is studied	A methodology for parameter extraction of statistical process variations in regard to FinFET is presented.
[80]	FINFET/ 25nm	TCAD	4T v/s 6T	RSNM, WSNM	This paper discusses the cell stability of 4T and 6T SRAM cells in subthreshold region.
[81]		TCAD	Un doped SOI-FinFET, Un doped SSOI FinFET and PDSOI FinFET	FOM, Cell stability, Write ability, Data Retention Value, Standby power, Short circuit current	If the tensile strain of SSOI substrates is relaxed for PFET channels then improved SRAM cell can be designed.
[82]	FINFET/ 22nm	Not Mentioned	9T SRAM	Area, Read stability, Write stability, Delay, Energy consumption, Standby leakage power, Sensing yield, Minimum required boosted WL voltage	Novel Power Gated 9T SRAM reduces the energy consumption.
[83]		Cadence Virtuoso	11T SRAM & 13T SRAM	Delay, Leakage Power, Area, DC/Tran Analysis	ST 11T (CMOS), ST 13T (FinFET), Power Gating.
[84]		Not Mentioned	9T SRAM	Read Stability, Write Ability, Power Consumption, Area, Novel Yield Estimation Method	Near Threshold 9T SRAM Cell reduces standby power and energy. In this paper a new yield estimation method is introduced.
[85]		2D Sentaurus Device Simulator	6T SRAM	Stability, Static Power, Area	Dynamic Back Gate design for Pull Up Transistors of SRAM. **1)** ABG with tied gate pullup. **2)** ABG with independent gate pull up.
[86]		Synopsys Taurus	6T SRAM	Cell read stability and write ability	1. 6T SRAM with PGFB (Pass Gate Feedback) 2. 6T SRAM with PUWG (Pull Up Write Gating).
[87]		HSPICE	Existing FinFET technologies & 6T SRAM	Hold stability, write ability and standby leakage current	To improve hold stability, various design method are proposed.
[88]	FINFET/ 20/16/14/1 0/7nm	HSPICE	7T SRAM	Write speed, Stability, Static power consumption, Area	To improve read-write stability, high & low voltage transistors are used.
[89]	FINFET/ 14nm	Not Mentioned	7T SRAM	Read access time, Energy and Power	NTV (Near Threshold Voltage) 7T SRAM Cell provides improved read access time, standby power and energy
[90]		TCAD	8T SRAM compared with previously reported 6T and 8T SRAM	RSNM, WM, Read Current, Leakage current	the write ability of the proposed cells can be improved with write-assist techniques,

Continued Table 2. Review summary of various FinFET based SRAM cell designs.

Ref.	Device/ Technology	Software Used	Technique	Parameters Worked on by the Authors	Remarks
[91]		TCAD	6T SRAM	Hold and read SNM, Read write access time, Standby leakage power	SymD-k structure improves device & circuit performance.
[92]	FINFET/ 12nm	3D TCAD	Multi-Gate transistor design inserted oxide (iFinFET)	IOFF v/s ION, C gg v/s C gd, Intrinsic delay, Process Induced Variations, Intrinsic Gain, Transfer char, Output char	iFinFET provides improved electrostatic integrity compared to FinFET.
[93]		3D TCAD	iFinFET (Inserted Oxide multi gate) design is compared against bulk FinFET and GAA FET (Gate All Around FET)	Ion, I_{OFF}, I eff ,DIBL	iFinFET is a promising device for low power applications as it provides improved cell performance with minimum complexity.
[94]	FINFET/ 10nm	Quantum physics-based NEMO5 simulator	6T SRAM	Access time, leakage power	Focusses on challenges of FinFET at 10 nm technology node.
[95]		TCAD	6T & 8T SRAM	Read static noise margin(RSNM),word-line write margin, and leakage	To improve RSNM, the pull down transistor fins are increased which results in increased area & leakage.
[96]	FINFET/ 7/8nm	3D TCAD	6T SRAM	Read Stability, Write ability, Butterfly curves, N curves, Ids-VDS char, Impact of systematic sources of variation, Area	6T SRAM: 1) control FinFET. 2) SSR (Super Steep Retrograde) FinFET.
[97]		3D TCAD	6T SRAM	Read Stability, Write ability, Butterfly curves, N curves, Ids-VDS char, Impact of systematic sources of variation, Area	6T SRAM: 1) control FinFET. 2) SSR (Super Steep Retrograde) FinFET.
[98]		3D TCAD	6T SRAM	Static noise margin, Standby leakage, Static power, V_{min}, Write margin yield	In active mode, the proposed device leads to significant leakage current.

Table 3. Review summary of various CNTFET based SRAM cell designs.

Ref.	Device/ Technology	Software Used	Technique	Parameters Worked on by the Authors	Remarks
[53]	CNTFET/ Not Mentioned	Nano HUB Tools	Oxide thickness variation	Leakage & Propagation delay	Performance is degraded in single & double gate MOSFET whereas CNTFET and nanowire FET offer less leakage & propagation delay.
[58]	CNTFET/ Not Mentioned	Not Mentioned	Spatial distribution	SNM & Current	Performance of CNTFET is varied due to spatial distribution of CNT.
[100]		SPICE	14T/ 8T SRAM	Delay & power of read/write operations	Delay for both designs is comparable
[101]	CNTFET/ 32nm	HSPICE	8T CNTFET SRAM	Static & dynamic power, Noise margin	Two approaches to overcome the presence of metallic CNTs; are presented & discussed.
[102]		HSPICE	8T CNTFET SRAM	Energy, delay, EDP, leakage current & SNM	Near Vth has its impact on these parameters. Furthermore, to improve performance & yield, word line boosting technique is explored.

Table 4. Review summary of various TFET based SRAM cell designs.

Ref.	Device/ Technology	Software Used	Technique	Parameters Worked on by the Authors	Remarks
[60]	TFET/ 25nm	TCAD	7T Driver less SRAM	Stability, Performance	The proposed cell provides improved hold, write, read stability & performance.
[61]	TFET/ 30nm	TCAD	6T SRAM	SNM, Delay, Off current & I_D-V_G	In order to address the unidirectional current limit of TFET, templates having better characteristics are used.
[64]	TFET/ 22nm	TCAD	10T HTFET SRAM & 6T FinFET SRAM	RSNM & Sidewall roughness variation	A comparative study of side wall roughness & variation effects in TFET & FinFET has been studied.
[103]	TFET/ 45nm	TCAD/HSPICE	7T H-TFET (Hetero-junction TFET) SRAM	Read/write SNM, delay & standby power	7T H-TFET SRAM cell shows reduced read delay time.
[104]	TFET/ 32nm	TCAD	8T & 6T TFET SRAM	Energy efficiency, leakage, cell area & access time	Due to less leakage, TFET SRAM has utilization for low standby power applications like IoT.
[105]	TFET/ 30nm	TCAD	6T DG-TFET SRAM	Cell area, delay & power consumption	To reduce the soft error sensitivity, RHBD (Radiation Hardened By Design) technique is implemented with a RC f/b loop.
[106]	TFET/ 22nm	TCAD	Mixed TFET-MOSFET 8T SRAM	Stability(H/R/WSNM)	TFET-MOSFET cell provide better stability at ultralow voltage operations.
[107]		TCAD	Si/Ge TFET SRAM & eDRAM (Embedded DRAM)	Standby power, area & performance (stability)	TFET based bit cells suffer area penalty due to higher number of transistors.
[108]	TFET/ 20nm	TCAD	12T TFET SRAM	Static power consumption, R/W/HSNM, area & write power consumption	A reverse bias current eliminated SRAM cell is proposed which is a promising candidate for ultralow power applications
[109]	TFET/ 10nm	Cadence/ HSPICE	TFET 6T SRAM (PU:PD:PG) & FinFET 6T SRAM	Stability, standby leakage power & W/R/HSNM	T-SRAMs have better HSNM & RSNM whereas F-SRAMs have better WSNM
[110]	TFET/ Not Mentioned	TCAD	6T TFET SRAM	Butterfly curves to assess cell stability & functionality	Half SRAM (HSRAM) based on strained silicon nanowire complementary TFET is fabricated & calibrated.
[111]	TFET/ Not Mentioned	TCAD/HSPICE	7T DP-DG TFET (Dual Pocket Double-Gate TFET) SRAM	Read stability, write ability, cell stability, read/write delay, power consumption & write margin	The poor drive current & Uni-directionality are the two challenges for deploying TFETs in SRAMs

5 respectively, keeping in view the technology node implemented, software used for simulation, various techniques opted for SRAM design and parameters worked on by the authors.

CONCLUSION

In conclusion, it is seen that much of the work has been done on SRAM cell by different authors. The work done so far is mostly related to improve the performance of SRAM design using different devices like MOSFET, FinFET, CNTFET and TFET. The performance has been improved in terms of SRAM stability, access time, leakage current, DIBL and Subthreshold Slope. Various SRAM design techniques have been used by the authors. Also, work has been done to calibrate and optimize the MOSFET, FinFET, CNTFET and TFET at different technology nodes to design a better SRAM cell. The simulations were done from few µms to 7nm technology node by different authors. HSPICE, TCAD, Synopsys Taurus and Cadence Virtuoso were some of the software used for simulation. The

Table 5. Summary of SRAM parameters worked on by various authors.

	CMOS SRAM	FinFET SRAM	CNTFET SRAM	TFET SRAM
Improved Leakage Current/ Power	[22], [28], [29], [31], [68], [69], [71]	[45], [46], [52], [74], [75], [76], [77], [91], [94]	[53], [102]	[103], [104]
Improved Read Stability	[20], [31], [65], [68] Reduced [29]	[44], [81]	[58]	[60], [61], [103]
Improved Write ability	[22], [28], [68]	[87]	[100], [101]	[60], [61], [103]
Improved Read Speed	Reduced [71]	[44], [89], [91]	[100], [102]	[103], [104], Degraded [61]
Reduced Delay/ Access time	Increased [69], [71]	[41], [81], [91], [94] Increased [52]	[53], [100], [101], [102]	Increased [105]
Improved Power/ Energy Consumption	[29], [69], [71]	[41], [44], [51], [74], [89]	[100], [101], [102]	[104], [105]
Better Stability (Hold/Read/Write SNM)	[65], [69], [71]	[51], [52], [75], [91]	[58], [101], [102]	[60], [61], [64], [103], [104]
Low DIBL	Not Discussed	[73], [77]	Not Discussed	Not Discussed
Steep SS	[69]	[73], [77]	Not Discussed	[104]
Reduced Cell Area	[29], Overhead [68], [71]	[44], [45]	Not Discussed	[108]
Improved EDP (Energy Delay Product)	Degraded [71]	[46]	[102]	[104]

advantages or the trade-offs of these techniques have been summarized in this paper. Thus, the review presented here will help researchers find the direction of research in the domain of SRAM cell design using emerging devices for low power applications in ultra-deep sub-micron technology.

CONFLICT OF INTEREST

Authors have no conflict of interest.

AUTHOR CONTRIBUTIONS

Writing-Original Draft Preparation, Editing, S. Ruhil; Review & Editing, V. Khanna, U. Dutta; Administrative Support, N. Shukla. All authors have read and agreed to the submitted version of manuscript.

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