A New Frequency Compensation Technique in Three Stage Amplifiers with Active Feedback

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ABSTRACT:
This paper presents a dual-active capacitance in reversed nested Miller compensation (DACRNMC) technique for low-voltage and large capacitive load amplifiers. The frequency bandwidth of the DACRNMC amplifier has been improved due to the usage of active compensation capacitors. The amplifier's die area is reduced in compare to the existing techniques in the RNMC scheme. The architecture also generates two left half plane zeros to increase the phase margin. The simulation for the proposed DACRNMC amplifier with a 0.18µm standard CMOS process reveals a unity gain bandwidth of 17.4MHz and phase margin of 64 degrees , while 500 pF load is driven from a single 1.5 V power supply.

KEYWORDS: CMOS Multistage Amplifiers, Nested Miller Compensation, Active Capacitive Feedback.

1. INTRODUCTION

Nowadays, with the device sizes scaling down and the reduction of supply voltages in sub-micron CMOS technologies, multistage amplifiers, widely used in the analogue and mixed signal circuits for the conventional cascade topologies, are not suitable for low voltage operations due to their less voltage swing and output impedance. In contrast, if no frequency compensation technique be employed, multistage amplifiers will have additional frequency poles and zeros resulting in inherently instability and reduced signal bandwidth.

There are generally two different compensation schemes in the three-stage amplifiers: Nested Miller Compensation (NMC) and Reversed Nested Miller Compensation (RNMC) [1-5]. An RNMC amplifier usually has a higher bandwidth than the NMC amplifier since in the RNMC amplifier the inner compensation capacitor does not load the amplifier's output. However, the RNMC scheme has a stability problem because of the appearance of a right half plane (RHP) zero in its frequency response. To alleviate this problem, many RNMC techniques have been reported to avoid the RHP zero such as the RNMC amplifier with voltage buffer and nulling resistor [1], reversed active feedback frequency compensation (RAFFC) [2], RNMC with voltage buffer and resistor [3], RNMC techniques with current follower (CF) and voltage follower (VF) [4], [5].

In this paper, a novel frequency compensation technique referred as the dual-active capacitance in reversed nested Miller compensation (DACRNMC) is proposed for three-stage amplifiers. This scheme of compensation uses two active compensation capacitors and yields a higher amplifier bandwidth.

The paper is organized as follows. In Sect. 2, the proposed DACRNMC amplifier is described. The circuit implementation of the proposed amplifier and its circuit level simulation results are presented in Sect. 3. A comparison of the proposed amplifier with published compensation techniques is given in Sect. 4 and finally, Sect. 5 concludes the paper.

2. THE PROPOSED TECHNIQUE

In this paper, a new frequency compensation technique for three-stage amplifiers called the *dual-active capacitance in reversed nested Miller compensation* (DACRNMC) is proposed. In Figure 1 the basic block diagram applied in this technique is shown where g_{m1}, g_{m2}, and g_{m3} comprise the main three-stage amplifier. R_a is the output resistance of the

AC path and R_b is the input resistance of the current buffer stage. C_{m2} is the AC coupling capacitor and C_{m1} is the Miller capacitor. g_{ma} acts as the AC boosting path of the second stage to increase the high frequency gain. Besides, the structure has a current buffer stage, g_{mb}, which creates a high speed feedback path and improves the amplifier's bandwidth.

In the DACRNMC amplifier, there is no passive compensation capacitor. Besides, in this technique an AC amplifier is added in parallel with the second stage comprising two signal paths at the second stage. The first one is a DC path mainly applied to (or something) a high DC gain, and the other one is an AC path for boosting the high-frequency gain. Also, this topology has a current buffer that creates another high-speed feedback path. By using two high-speed paths, the non-dominant poles are shifted towards the high frequencies [7]. Consequently, the gain-bandwidth product or the unity-gain frequency of the amplifier is also improved.

Assuming that C_L, C_{m1} and C_{m2} >> C_i, and $g_{mi}R_i$, $g_{mf}R_L$ and $g_{mb}R_1$ >>1, and considering $g_{mb} \approx 1/R_b$, the small-signal transfer function of the DACRNMC amplifier can readily be obtained as given in relation (1) where $A_0 = g_{m1}g_{m2}g_{m3}R_1R_2R_3$ is the DC gain and ω_{P1} is the real dominant pole of the amplifier.

$$A_v(s) = A_0 \frac{1 + s\left(\frac{C_{m1}}{g_{mb}} + \frac{(g_{m2}+g_{ma})(R_a \parallel R_2)g_{m3}+g_{mf}}{g_{m2}g_{m3}}C_{m2}\right) + s^2\frac{(g_{m2}+g_{ma})(R_a \parallel R_2)g_{m3}+g_{mf}}{g_{m2}g_{m3}g_{mb}}C_{m1}C_{m2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1 + s\frac{(g_{m2}+g_{ma})(R_a \parallel R_2)g_{m3}+g_{mf}}{g_{m2}g_{m3}}C_{m2} + s^2\frac{C_{m2}C_LC_1}{g_{m2}g_{m3}C_{m1}}\right]} \quad (1)$$

Suppose that $A_2(f)$ presents the overall gain at the second stage. Then, by neglecting the effect of the parasitic capacitances, the AC gain of the second stage can be obtained as follows:

$$A_{ac} = \lim_{f\to\infty} |A_2(f)| = (g_{m2}+g_{ma})(R_a \parallel R_2) \quad (2)$$

The dominant pole is

$\omega_{P1} \approx 1/C_{m1}g_{m2}g_{m3}R_1R_2R_3$

and the gain-bandwidth (GBW) is given by

$$GBW = A_0.\omega_{P1} = \frac{g_{m1}}{C_{m1}} \quad (3)$$

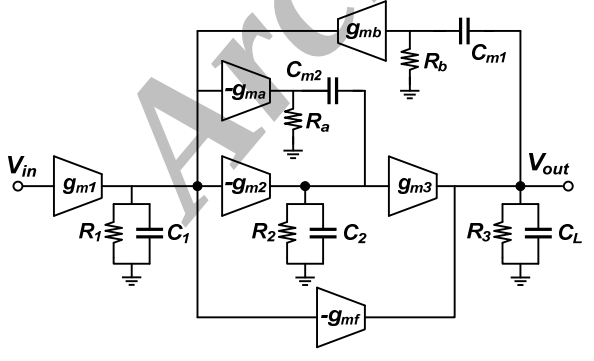

Fig. 1. Proposed dual-active capacitance compensation for the three-stage amplifier.

By assuming $g_{m3} = g_{mf}$, the slew rate of the DACRNMC amplifier is improved because in this case the output stage can be implemented as a AB fashion class and the small-signal transfer function is simplified as follows:

$$A_v(s) = A_0 \frac{1 + s\left(\frac{C_{m1}}{g_{mb}} + \frac{A_{ac}+1}{g_{m2}}C_{m2}\right) + s^2\frac{A_{ac}+1}{g_{m2}g_{mb}}C_{m1}C_{m2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1 + s\frac{A_{ac}+1}{g_{m2}}C_{m2} + s^2\frac{C_{m2}C_LC_1}{g_{m2}g_{m3}C_{m1}}\right]} \quad (4)$$

From equation (4), the non-dominant poles and zeros are obtained as:

$$\omega_{Z1} = -\frac{g_{mb}}{C_{m1}} \quad (5)$$

$$\omega_{Z2} = -\frac{g_{m2}}{(A_{ac}+1)C_{m2}} \quad (6)$$

$$\omega_{P2,3} = -\frac{(A_{ac}+1)g_{m3}C_{m1}}{2C_1C_L}\left(1 \pm j\sqrt{\frac{4g_{m2}C_1C_L}{g_{m3}C_{m1}C_{m2}(A_{ac}+1)^2} - 1}\right) \quad (7)$$

It is seen that, the proposed three-stage amplifier has one real dominant pole, two complex non-dominant poles, and two left half plane zeros. All zeros in the DACRNMC amplifier are located at the left half plane resulting in improved phase margin, hence, the unity gain bandwidth. The pole-zero diagrams of uncompensated and DACRNMC amplifiers are illustrated in Figure 2.

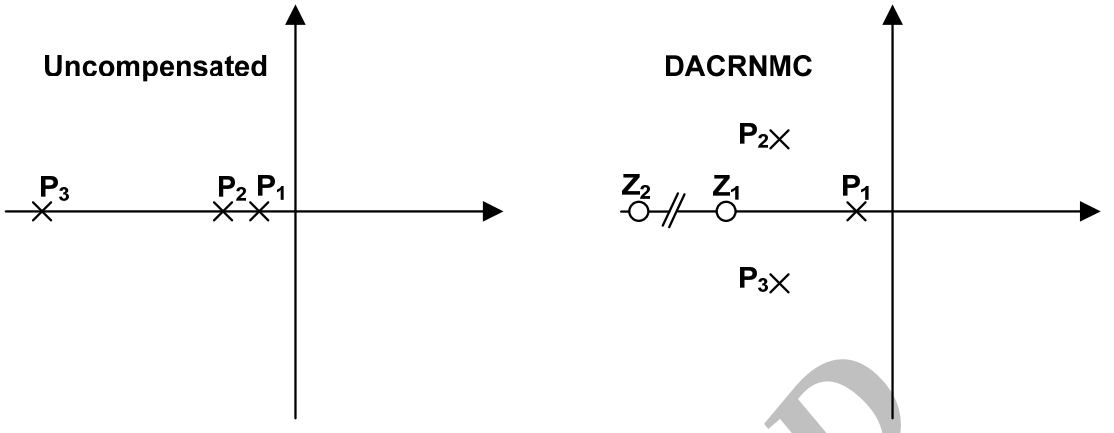

Fig. 2. Pole-zero diagrams of Uncompensated and DACRNMC compensated amplifiers.

The AC boosting gain, A_{ac}, plays a critical role in the amplifier's design since by increasing A_{ac}, the non-dominant poles are shifted to a higher frequency so that the phase margin is enhanced.

By using a third-order Butterworth response in order to arrange the non-dominant poles of the DACRNMC amplifier similar to the one described in [9], the values of compensation capacitances, C_{m1} and C_{m2}, are given by

$$C_{m1} = 2\sqrt{\frac{g_{m1}C_L C_1}{g_{m3}(1+A_{ac})}} \tag{8}$$

$$C_{m2} = g_{m2}\sqrt{\frac{C_L C_1}{g_{m1}g_{m3}(1+A_{ac})^3}} \tag{9}$$

It is seen that from (8) and (9), for a given transconductance for the main gain stages and load capacitance, the values of compensation capacitors, C_{m1} and C_{m2}, are decreased as a result of an increment of A_{ac}. Therefore, by increasing the AC boosting gain, the total die area of the amplifier can be decreased.

Since in the small signal relation of the amplifier given in (1) the order of the numerator is less than the denominators, thus the stability is determined by the denominator. Whereas by applying the Routh-Hurwitz stability criterion as described in [2] on the characteristic equation (1), we can obtain the stability condition as follows:

$$GBW < \frac{g_{m3}(1+A_{ac})}{C_L C_1} C_{m1} \tag{10}$$

By replacing C_{m1} from relation (8) into (10), the stability condition of the DACRNMC amplifier is also equivalent to:

$$GBW < 2\sqrt{\frac{g_{m1}g_{m3}(1+A_{ac})}{C_L C_1}} \tag{11}$$

According to (11), for a given load capacitance, C_L, the GBW will be increased if the transconductance of the first and third stages, g_{m1} and g_{m3}, or the AC boosting parameter, A_{ac}, is increased. Since increasing g_{m1} or g_{m3} results in higher power dissipation, the latter option should be preferred. Thus, A_{ac} is the best parameter in order to boost the GBW, decrease the die area, and to move the non-dominant poles towards the high frequency.

3. DESIGN CONSIDERATIONS AND SIMULATION RESULTS

To prove the effectiveness of the proposed compensation technique, HSPICE simulations are carried out using a 0.18-µm BSIM3v3 level 49 CMOS technology. The amplifier was designed to achieve a DC gain of about 100dB and a phase margin of 60° with a capacitive load of 500 pF and a 1.5-V power supply.

The circuit implementation of the three-stage DACRNMC amplifier is presented in Figure 3. The first gain stage is realized by transistors M0–M8 with a pMOS input differential pair which is made up of a folded cascade amplifier. The second inverting stage is built of a common source amplifier with an active load, M9-M10. The last non-inverting stage is realized by transistors M11-M14.

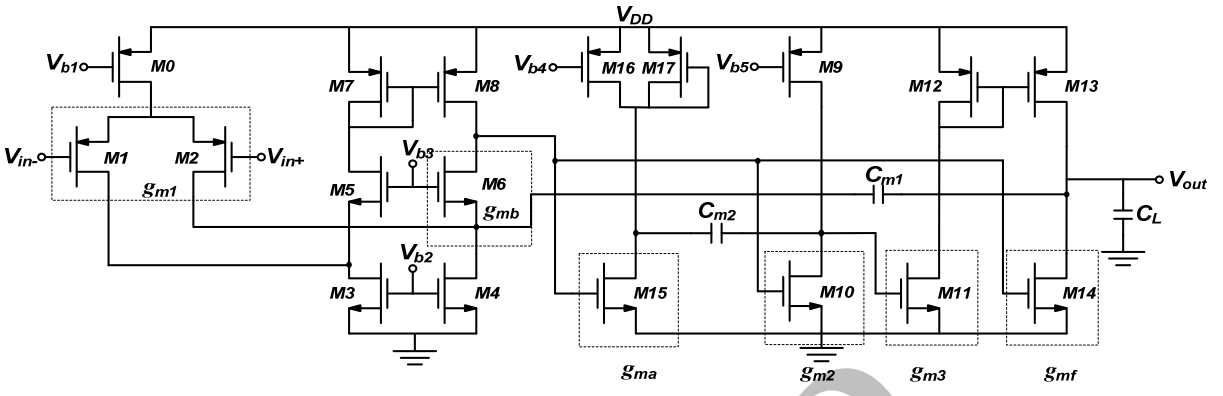

Fig. 3. Circuit implementation of a three-stage amplifier.

Moreover, the g_{mb} compensation stage is simply configured by transistor M6 of the folded cascode input stage amplifier, whereas M15 to M17 act as the AC boosting stage. At the AC boosting stage, the transistor M17 is used to determine the DC common mode voltage at the drain of M15. Finally, the feedforward transconductance stage, g_{mf}, is realized by M14.

Table 1. Circuit PARAMETERS

Parameter	Value
M0	2×(6.6/0.36)
M1, M2	6/ 0.36
M3, M4	2×(3/ 0.36)
M5, M6	3/ 0.36
M7, M8	1.2/0.36
M9	5×(5.4/0.36)
M10	2/ 0.36
M11, M14	2/ 0.36
M12, M13	9/ 0.36
M15	2 / 0.36
M16	3×(5.1/ 0.36)
M17	2×(5/ 0.36)

The parameter values of the designed circuit for the proposed amplifier are presented in Table 1. By using (2), the value of A_{ac} is set at about 9, and according to (8), the Miller capacitance C_{m1} can be 1.2 pF. From (9), we get the Miller capacitance C_{m2} of 0.2pF. In order to achieve the targeted gain-bandwidth product, g_{m1} is set to 97µA/V. And also g_{mb}=205 µA/V, g_{ma}=354 µA/V, g_{m2}=345 µA/V and g_{m3}=g_{mf}=352 µA/V.

Figure 4 shows the simulated open-loop frequency response of the proposed amplifier. The large signal and small signal transient responses of the amplifier in a unity-gain negative feedback configuration are shown in Figs. 5 and 6, respectively. In the large signal transient simulation an input step of 400-mV was applied whereas in the small signal transient simulation the amplitude of the input signal was 40-mV. The resulting DC gain, unity gain-bandwidth and phase margin are equal to 98dB, 17.4MHz and 64°, respectively. The total power current consumption is 200µA. Table 2 summarizes the simulation results of the proposed three stage amplifier.

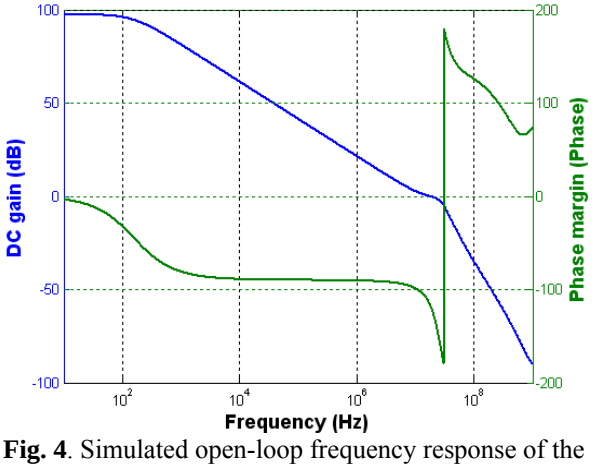

Fig. 4. Simulated open-loop frequency response of the amplifier.

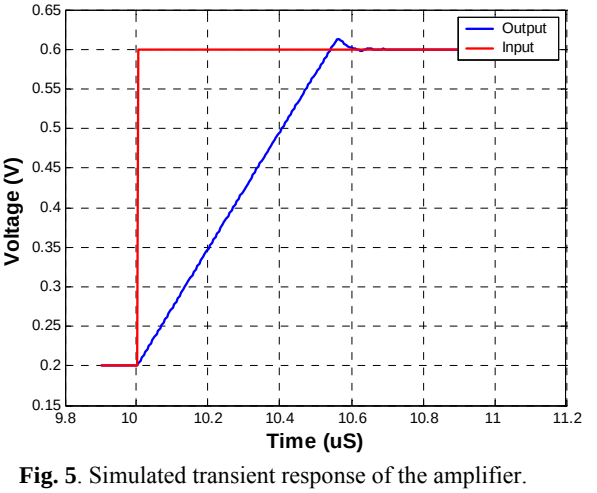

Fig. 5. Simulated transient response of the amplifier.

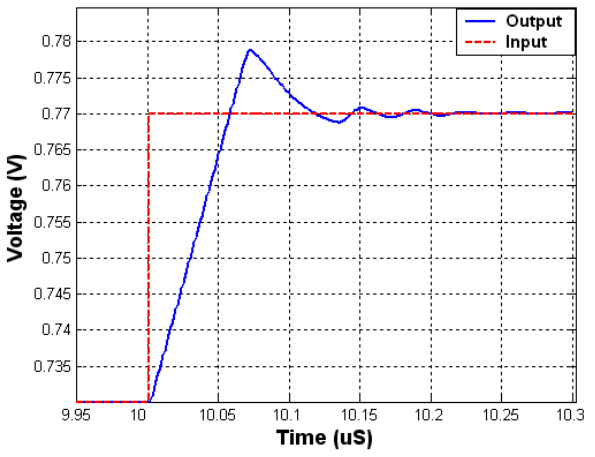

Fig. 6. Small-signal input-output characteristic of the amplifier.

Table 2. Performance Summary of Simulated Amplifier

Parameter	Value
Gain (dB)	98
GBW (MHz)	17.4
Phase Margin (degree)	64
Power (µW)	300
Total Current (mA)	0.2
T_S (µs) +/–	0.6/0.5
SR (V/µs) +/–	0.7/0.95
SR (V/µs) (average)	0.825
C_{m1} (pF)	1.2
C_{m2} (pF)	0.2
V_{DD} (V)	1.5
C_L (pF)	500
Technology	BSIM3v3 Level 49 0.18-µm CMOS

Table 3. Comparison of different multistage amplifiers

	C_L (pF)	V_{DD} (V)	I_{TOT} (mA)	Power (µW)	GBW (MHz)	SR (V/µs)	Capacitor (pF)	FOM_S (MHz×pF/mW)	FOM_L (V/µs×pF)/mW	$IFOM_S$ (MHz×pF)/mA	$IFOM_L$ (V/µs×pF)/mA	Technology µm-CMOS
RNMCVBNR [1]	15	3	0.48	1.44	19.46	13.8	C_{m1}=3 C_{m2}=0.7	209	149	608	430	-
AFFC [6]	120	2	0.2	0.4	4.5	1.49	C_{m1}=5.4 C_{m2}=4	1350	447	2700	894	0.8 µm
ACBCF [7]	500	2	0.162	0.324	1.9	1.0	C_{m1}=10 C_{m2}=3	2932	1543	5864	3086	0.35 µm
SMFFC [8]	120	2	0.21	0.42	9	3.4	C_m=4	2571	971	5143	1943	0.5 µm
PFC [9]	130	1.5	0.19	0.275	2.7	1.0	C_{m1}=15 C_{m2}=3	1276	473	1915	709	0.35 µm
DLPC [10]	120	1.5	0.22	0.33	7.0	3.3	C_{m1}=4.8 C_{m2}=2.5	2545	1200	3818	1800	0.6 µm
[14]	500	1.5	0.15	0.225	1.4	2.0	C_{m1}=30 C_{m2}=20	3111	4444	4666	6666	0.35 µm
AFCB [15]	120	1.5	0.058	0.088	8.5	3.4	C_{m1}=0.9 C_{m2}=0.3	11590	4636	17586	7034	0.18 µm
RNMC-VB-OR [16]	500	3	0.083	0.249	2.87	1.55	C_{m1}=10 C_{m2}=0.3	5764	3112	17289	9337	0.5 µm
DACRNMC	**500**	**1.5**	**0.2**	**0.3**	**17.4**	**0.825**	**C_{m1}=1.2 C_{m2}=0.2**	**29000**	**1375**	**43500**	**2062**	**0.18 µm**

4. PERFORMANCE COMPARISON

It is difficult to make accurate evaluations on different amplifiers that are implemented with different technologies for different operating purposes. However, to provide a clearer picture of the improvement by the proposed topology, a comparison of some published compensation topologies with the prepared topology in this paper is shown in Table 3. To evaluate different amplifiers two figures of merit were proposed to characterize small-signal (GBW) and large-signal (slew rate) performances of the amplifier and are given by [11, 12].

$$FOM_S = \frac{GBW \times C_L}{\text{Power}} \quad (12)$$

$$FOM_L = \frac{SR \times C_L}{\text{Power}} \quad (13)$$

By using these formulas, the value of higher FOM shows the better performance of the amplifier. However, when the supply voltages differ, using these formulas for evaluation is relatively rough, since the GBW and the SR are directly related to quiescent currents flowing in the relevant transistors. In order to achieve a more precise comparison two new formulas are provided, given by [7], [13]

$$IFOM_S = \frac{GBW \times C_L}{I_{dd}} \quad (14)$$

$$IFOM_L = \frac{SR \times C_L}{I_{dd}} \quad (15)$$

Obviously, the measured results show that the proposed amplifier has significantly outperformed all the other referenced amplifiers.

5. CONCLUSIONS

In this paper, a new compensation technique called DACRNMC for three stage amplifiers has been presented. It has been shown that a larger bandwidth compared to the other reported topologies can be obtained without using any passive compensation capacitors. Furthermore, by employing the active compensation capacitors, the die area of the circuit, which is mainly occupied by the compensation capacitors, has been significantly reduced. The proposed compensation technique achieves larger FOM_S and $IFOM_S$ compared to other compensation topologies reported previously.

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