A New Zero Voltage Switching Buck-Boost Type DC-DC Converter

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ABSTRACT:
In this paper we proposed, a new zero voltage switching isolated buck-boost DC-DC converter with active clamp circuit. The active clamp circuit in this converter not only absorbs voltage spikes across the main switch but also provides soft switching conditions for all switches. All switches are Pulse Width Modulation controlled which simplifies the control implementation. One of the main advantages of this converter is operating at high power levels while soft switching conditions exist in both buck and boost modes of converter operation. Since this converter can operate over a wide input voltage range, it can be employed in power factor correction. The experimental results obtained from a 150W prototype circuit operating at 100 KHz are presented to confirm the integrity of the proposed circuit.

KEYWORDS: Active Clamp, Soft Switching, Pulse Width Modulation, Buck-Boost, Fly Back Current.

1. INTRODUCTION

DC-DC converters are vastly used in industrial applications [1 - 5]. Modern power supplies require high circuit efficiency and high power density. Increasing the switching frequency can reduce the weight and size of the passive component but the switching losses in power switches will increase accordingly.

The soft switching techniques with variable switching frequencies such as resonant converters reduce switching losses [6 - 7], but they have complex control circuit and their magnetic component's values are not optimum. The asymmetrical pulse width modulation techniques are proposed to achieve the zero voltage (ZV) condition at the turn on instance but in these converters, the switching voltage and current stresses are related to the duty cycle [8]. Full bridge converters with phase shift pulse width modulation provide ZV condition for power switches but the soft switching range for lagging leg switches is narrow. The active clamp techniques [9 - 11], provide ZV condition at the turn on instant. An active clamp circuit can recycle the leakage inductance energy with minimal voltage stress to the main switch.

In this paper an active clamp circuit is applied to a single switch flyback current-fed converter. The proposed converter has only two power switches (main and auxiliary). This converter has both characteristics of buck and boost converters in a single power stage of conversion. Therefore it can operate over a wide input voltage range and can be used as a power factor correction. The proposed converter operates under the ZV condition in both buck and boost modes. Since this converter is controlled by the PWM scheme, the control implementation is simple. Therefore the proposed converter performs at a higher efficiency than hard switching counterpart [5].

The circuit configuration and operational principle of the proposed converter is illustrated in section 2. In section 3, the steady state analysis is presented and in section 4 the design procedure is described. The simulation experimental results obtained from the proposed converter Prototype are presented in section 5 which verifies the theoretical analysis.

2. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

2.1. Circuit Configuration

The proposed flyback current-fed converter with active clamp circuit is shown in Fig. 1. In this converter, D_1-D_3 are output diodes and L_{m1},L_{m2} are magnetizing inductors of the flyback and the forward

transformer respectively. S and Sa are the main and auxiliary switches and C_b and C_o are the blocking and output capacitor of the converter. L_K is the leakage inductor of the transformers and C_S and C_a are the snubber capacitors of the main and auxiliary switches. The active clamp circuit which includes S_a and C_c, not only provides ZVS condition for all switches, but also limits the peak voltage stress of the main switch S. Inherently, this converter can operate at a higher power level than a flyback or an equivalent forward converter. Furthermore, the active clamp circuit provides ZV condition for both switches at turn on and the soft switching at turn off. Therefore the proposed converter operates with a higher switching frequency and the size of the passive components is reduced.

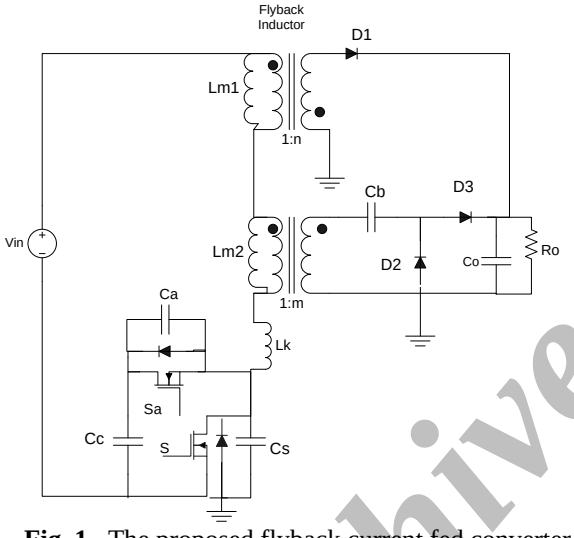

Fig. 1. The proposed flyback current fed converter with an active clamp circuit

2.2. Operational Principle

In order to simplify the steady state analysis, the following assumptions are made.

All parasitic components are neglected except L_K

The clamp capacitor is large enough, so V_{Cc} (clamp capacitor voltage) is constant in a switching cycle

L_{m1} and L_{m2} are large enough

The energy stored in the leakage inductance just before switch turn on is greater than energy stored in the snubber capacitors in order to achieve ZVS operation.

The proposed circuit has ten distinct operating modes in one period. The main waveforms of the proposed converter are presented in Fig. 2.

Before the first mode, the main switch is on and the current through L_{m1} is linearly increasing and D_3 is also conducting. The equivalent circuit for each operating interval of the proposed converter is shown in Fig. 3.

Mode1 (t_0-t_1): This mode starts with the main switch S turning off, hence the L_{m1} and L_{m2} currents charge C_s and discharge C_a, linearly. When C_s voltage reaches V_{C1}, D_1 turns on and this mode ends, thus:

$$V_{C1} = V_{in} - \frac{V_{Cb}}{m} + V_O\left(\frac{1}{n} - \frac{1}{m}\right) \quad (1)$$

Mode2 (t1-t2): In this mode the leakage inductance current continues to charge C_s until its voltage reaches V_{Cc} and discharges C_a to zero simultaneously. Then, the anti-parallel diode of S_a conduct and prevent V_{Ca} to go negative. The duration of this mode is very small and can be neglected in a switching period. The voltages across L_{m1} and L_{m2} are as following:

$$V_{Lm1} = -\frac{V_O}{n} \quad (2)$$

$$V_{Lm2} = \left(\frac{V_O - V_{Cb}}{m}\right) \quad (3)$$

Mode3 (t_2-t_3): While D_a is conducting, the auxiliary switch Sa, can be turned on under ZV condition and I_{LK} starts to decrease with a constant slope. This mode ends when I_{LK} is reduced to I_{Lm2}.

$$V_{LK} = V_{in} + V_O\left(\frac{1}{n} - \frac{1}{m}\right) + \frac{V_{Cb}}{m} \quad (4)$$

Mode4 (t_3-t_4): When I_{LK} reaches I_{Lm2}, D_2 begins to conduct and D_3 is turned off. This mode continues until I_{LK} reaches zero. Important relations for this mode are as following:

$$V_{LK} = V_{in} + \frac{V_O}{n} + \frac{V_{Cb}}{m} - V_{Cc} \quad (5)$$

$$V_{Lm1} = -\frac{V_O}{n} \quad (6)$$

$$V_{Lm2} = -\frac{V_{Cb}}{m} \quad (7)$$

Mode5 (t_4-t_5): When leakage inductance current changes direction and becomes negative, this current transfers from D_a to S_a, and the clamp capacitor starts to discharge. This extra current with respect to hard switching is imposed on D_1 and D_2. I_{LK} slope in this interval is the same as in the previous mode.

Mode6 (t_5-t_6): This mode begins when S_a is turned off and I_{LK} discharges C_s and charges C_a. This modes ends when C_a is charged to V_{Cc}.

Mode7 (t_6-t_7): The anti_parallel diode of the main switch begins to conduct and prevents the voltage of C_a to go negative, and I_{LK} decreases in magnitude. During this mode the main switch can be turned on under zero voltage zero current (ZVZC) condition. This mode ends when I_{LK} reaches zero.

$$V_{LK} = V_{in} + \frac{V_O}{n} + \frac{V_{Cb}}{m} \quad (8)$$

Mode8 (t_7-t_8): This mode starts, when I_{LK} becomes positive and its current flows through the main switch.

I_{LK} increases with the same slope as in the previous mode. This interval ends when I_{LK} reaches I_{Lm2}.

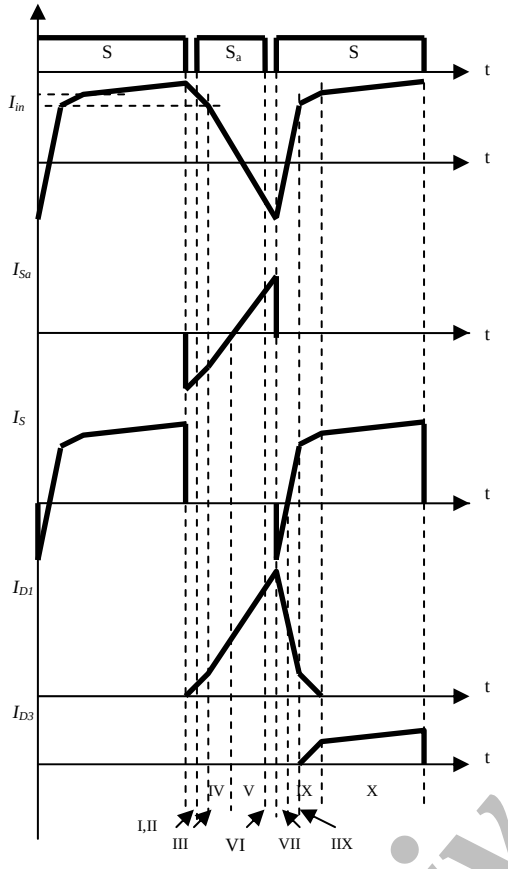

Fig. 2. Main waveforms of the proposed converter

Mode9 (t_8-t_9): When I_{LK} reaches I_{Lm2}, D_2 turns off and D_3 turns on, thus both diodes are softly switched. V_{Lm1} and V_{Lm2} are expressed in (9), (10). In this mode, I_{LK} increases with a new slope (V_{LK}/L_{LK}) as can be observed from (11).

$$V_{Lm1} = -\frac{V_O}{n} \tag{9}$$

$$V_{Lm2} = (\frac{V_O - V_{Cb}}{m}) \tag{10}$$

$$V_{LK} = V_{in} - \frac{V_{Cb}}{m} + V_O(\frac{1}{n} - \frac{1}{m}) \tag{11}$$

Mode10 (t_9-t_{10}):This mode begins when I_{LK} reaches I_{Lm1} and thus D_1 turns off under ZV condition and the leakage inductor current is equal to I_{Lm1}. Important relations for this mode are as following:

$$V_{Lm1} = V_{in} + \frac{V_{Cb}}{m} - \frac{Vo}{m} \tag{12}$$

$$V_{Lm2} = (\frac{V_O - V_{Cb}}{m}) \tag{13}$$

$$I_{Lm1} = \frac{V_{in} + \frac{V_{Cb}}{m} - \frac{Vo}{m}}{L_{m1}}(t - t_0) + I_0 \tag{14}$$

3. ANALYSIS OF THE PROPOSED CONVERTER

3.1. Voltage Conversion Ratio

In this section, for the convenience of the converter analysis, the dead times between the gating of main switch, S, and auxiliary switch, S_a, can be neglected. By writing the volt_second balance for T_2, Equ. 15 is obtained and from this relation V_{Cb} can be calculated as Equ. 16.

$$(1-D)T\frac{V_{Cb}}{m} = D_{loss}T(\frac{-V_{Cb}}{m}) + (\frac{V_O - V_{Cb}}{m})(D - D_{loss})T \tag{15}$$

$$V_{Cb} = (D - D_{loss})V_O \tag{16}$$

Where DT is the duration of modes 7 through 10 and $D_{loss}T$ is the duration of modes 7 through 9. Also the duration of modes 2 through 5 is (1-D)T.

V_{Cb} is the blocking capacitor voltage. In a similar way, the volt_second balance for flyback transformer can be expressed as Equ. 17 in order to calculate the voltage dc gain as Equ. 18.

$$(1-D)T.D_{loss}(\frac{V_O}{n}) = D_{loss}T(-\frac{V_O}{n}) + (V_{in} - \frac{V_O}{m} + \frac{V_C}{m})(D - D_{loss})T \tag{17}$$

$$\frac{V_O}{V_{in}} = \frac{(D - D_{loss})}{(1-(D - D_{loss})).(\frac{1}{n} + \frac{(D - D_{loss})}{m})} \tag{18}$$

The clamp capacitor voltage for the proposed converter is obtained by Equ. 19 and by substituting Equ. 16 and Equ. 18 into this relation, Equ. 20 is obtained.

$$V_{Cc} = V_{in} + \frac{V_O}{n} + \frac{V_C}{m} \tag{19}$$

$$V_{Cc} = \frac{V_{in}}{1-(D - D_{loss})} \tag{20}$$

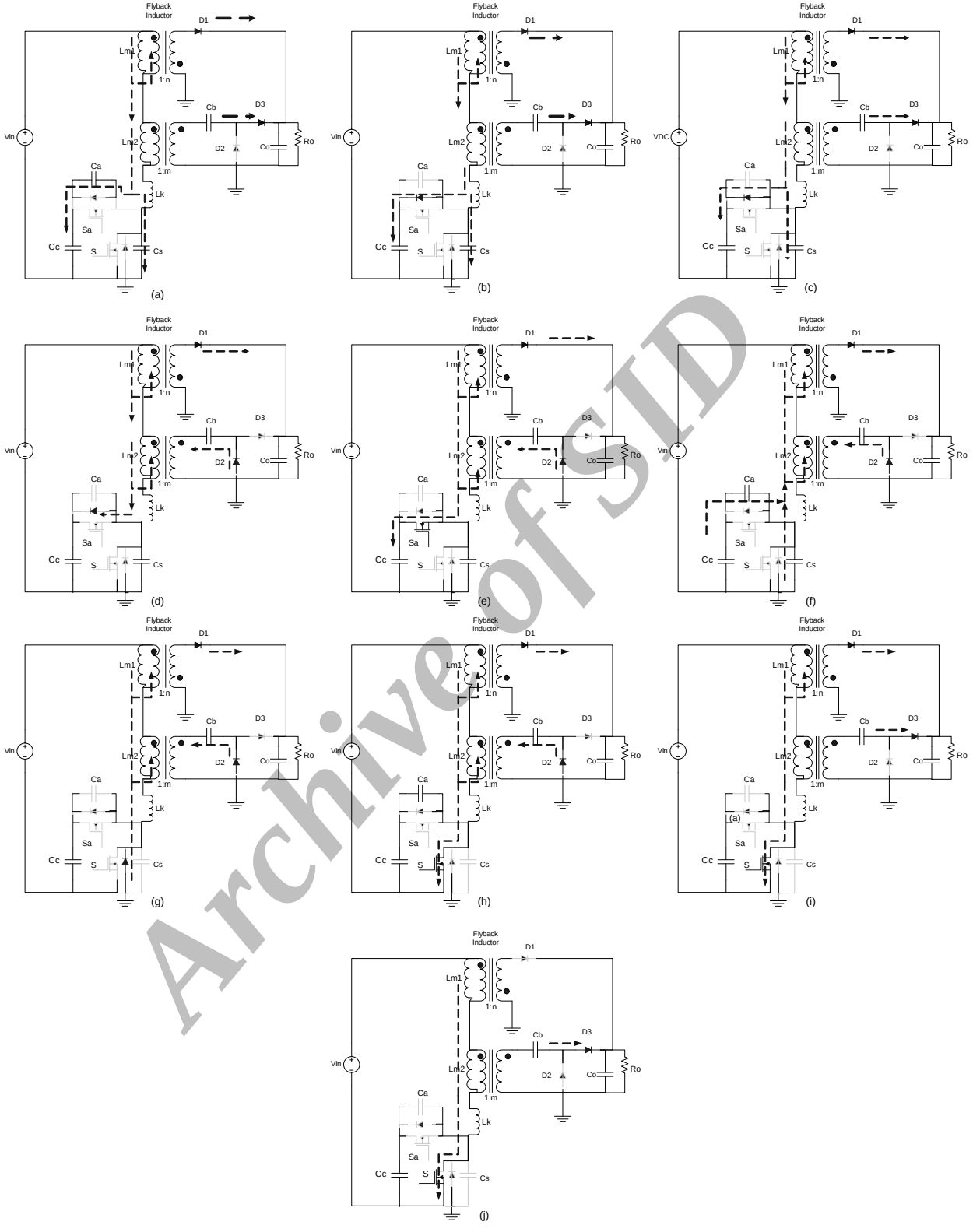

Fig. 3. The equivalent circuit for each operating interval of the proposed converter: (a)t0-t1, (b)t1-t2, (c)t2-t3, (d)t3-t4, (e)t4-t5, (f)t5-t6, (g)t6-t7, (h)t7-t8, (i)t8-t9, (j)t9-t10

3.2. Calculation of D_{loss}

Since the slopes of the flyback transformer current and the relating intervals are known in the 8th and 9th modes, D_{loss} can be calculated as a function of I_P. Thus

$$I_P \approx \frac{(1-D)T}{L_K}(V_{in} + \frac{V_O}{n} + \frac{V_{Cb}}{m} - V_{Cc}) \quad (21)$$

$$D_{loss} \approx \frac{I_P L_K . f}{V_{in}}.(1-D) \quad (22)$$

3.3. Stress of switching devices

The maximum voltage stress across the main switches and diodes can be obtained from Equ. 23 to Equ. 26.

$$V_S(\max) = V_{Sa}(\max) = \frac{V_{in}(\max)}{1-D_{eff}} \quad (23)$$

$$V_{D1}(\max) = mV_{in}(\max) + V_{Cb} = mV_{in}(\max) + D_{eff}.V_O \quad (24)$$

$$V_{D2}(\max) = \frac{V_{in}(\max).(1+\frac{n}{m}D_{eff}(1+D_{eff})}{(1-D_{eff}).(\frac{1}{n}+\frac{D_{eff}}{m})} \quad (25)$$

$$V_{D3}(\max) = \frac{\frac{m}{n}V_{in}(\max).(Deff\ -1) + D_{eff}.V_{in}(1+m)}{(1-D_{eff}).(\frac{1}{n}+\frac{D_{eff}}{m})} \quad (26)$$

Where D_{eff} is $D\text{-}D_{loss}$

3.4. Calculating the magnetizing inductors

During mode 10, the current ripple on the magnetizing inductor is obtained by Equ. 27. Thus, by rearranging Equ. 27, the magnetizing inductor can be calculated by Equ. 28.

$$\Delta i_{Lm1} \approx \frac{D_{eff}T(V_{in}(\min) - \frac{V_o}{m} + \frac{V_{Cb}}{m})}{L_{m1}} \quad (27)$$

$$L_{m1} \approx \frac{D_{eff}T(V_{in}(\min) - \frac{V_o}{m}(1-D_{eff}))}{\Delta i_{Lm1}} \quad (28)$$

Following a similar procedure, the following relations are obtained for L_{m2}.

$$\Delta i_{Lm2} \approx \frac{(1-D_{eff}).D_{eff}T\frac{Vo}{m}}{L_{m2}} \quad (29)$$

$$L_{m2} \approx \frac{(1-D_{eff}).D_{eff}T\frac{Vo}{m}}{\Delta i_{Lm2}} \quad (30)$$

3.5. Calculating The Clamp Capacitor

The general relation for clamp capacitor is provided by Equ. 31. By substituting $\Delta V_{Cc} = 0.1V_{Cc}$ and using (20), we can obtain (32).

$$C_c = \frac{\Delta t.I}{\Delta V} = \frac{(1-D_{eff}).T.I_P}{\Delta V_{Cc}} \quad (31)$$

$$C_c = \frac{10(1-D_{eff})^2 T.I_P}{V_{in}} \quad (32)$$

4. THE DESIGN PROCEDURE

To design the proposed converter, elements L_{m1}, L_{m2}, and C_c are selected according to Equ. 28, Equ. 30 and Equ. 32 respectively. Thus in order to provide a soft switching operation, only the values of the snubber capacitors should be calculated. First, it can be assumed that D_{loss} is zero and therefore V_{cb}, V_{Cc} and the peak current of flyback transformer (I_p) are calculated by Equ. 16, Equ. 20 and Equ. 21 respectively. Then, using the value of I_p, D_{loss} is calculated from Equ. 22 and the value of D can be corrected to $D+D_{loss}$ and 1-D can be corrected to $1-(D+D_{loss})$. According to the new value of D, the value of I_p is corrected and the energy of L_K before switch turn off can be estimated. Since this energy discharges the snubber capacitors, Equ. 33 is established and the snubber capacitor can be calculated.

$$\frac{1}{2}L_K(nI_P - I_{Lm1})^2 \geq \frac{1}{2}C_{eq}V_{Cc}^2 \quad (33)$$

Where C_{eq} is the sum of C_s and C_a.

5. EXPERIMENTAL & SIMULATION RESULTS

The simulation and experimental results are presented in this section to verify the effectiveness of the proposed converter. The realized prototype converter specifications are listed in Table 1 and the component list for practical implementation is shown in Table 2. Fig. 4 shows simulated voltage and current of the main switch in boost mode and Fig. 5 shows the simulated voltage and current of the auxiliary switch in boost mode. The implemented converter is shown in Fig. 6. Fig. 7 shows the measured waveform of drain-source voltage and current of the main switch to illustrate the ZVZC feature in boost mode. Also, voltage and current waveforms of the auxiliary switch in boost mode are shown in Fig. 8. It can be observed that the main switch and the auxiliary switch currents are negative before the turn on instant of switching devices. Therefore their body diodes are conducting and switches are turned on under ZVZC. Fig. 9 and Fig. 10 illustrate the measured results of drain-source voltage and current of the main and auxiliary switches in buck mode, respectively. It can be observed that the

soft switching condition at turn on instant also exist for the main and auxiliary switches in buck mode.

Table 1. Proposed converter specifications

Specifications	value
Input voltage	60V
Output voltage(boost)	110V
Output voltage(buck)	40V
frequency	100KHz
PO(Boost)	150W

Table 2. Power stage Components

Components	Part name/ value
S,S_a	IRF740
D_1-D_3	MUR460
L_{m1},L_{m2}	1mH
C_o	220uF
C_s	1nF
L_K	20uH
C_c	3uF
n,m	1:1

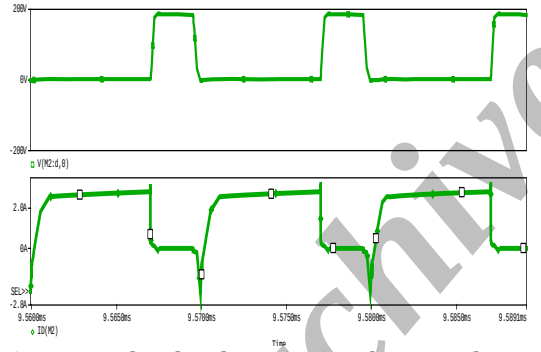

Fig. 4. Simulated Voltage (top) and current (bottom) waveforms of the main Switch in boost mode

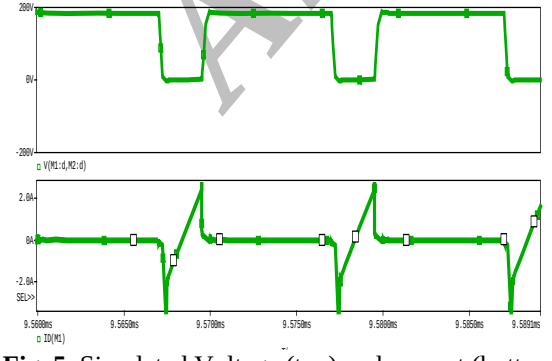

Fig. 5. Simulated Voltage (top) and current (bottom) waveforms of the auxiliary Switch in boost mode

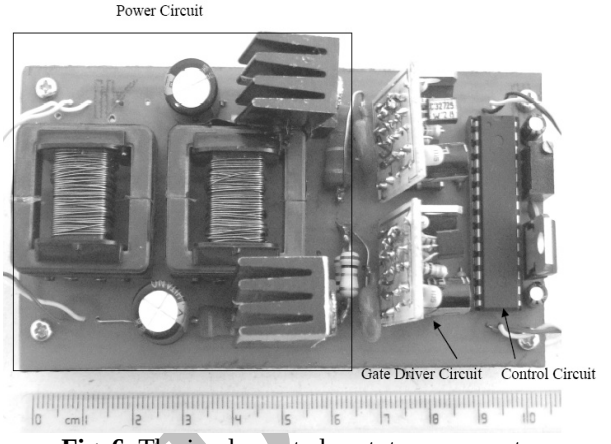

Fig. 6. The implemented prototype converter

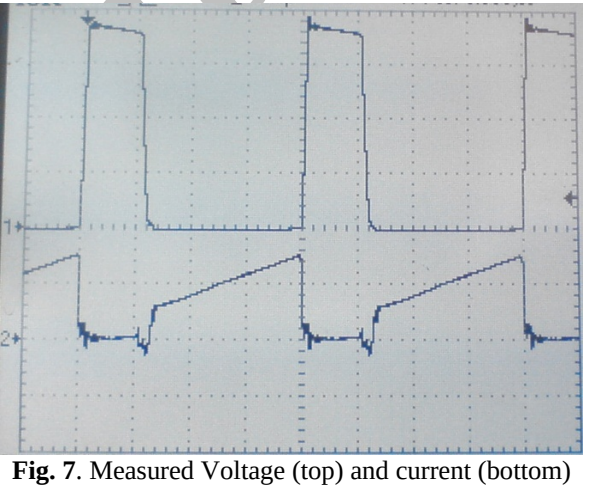

Fig. 7. Measured Voltage (top) and current (bottom) waveforms of the main Switch (vertical scale 60V/div or 5A/div, time scale 2.5µs/div)

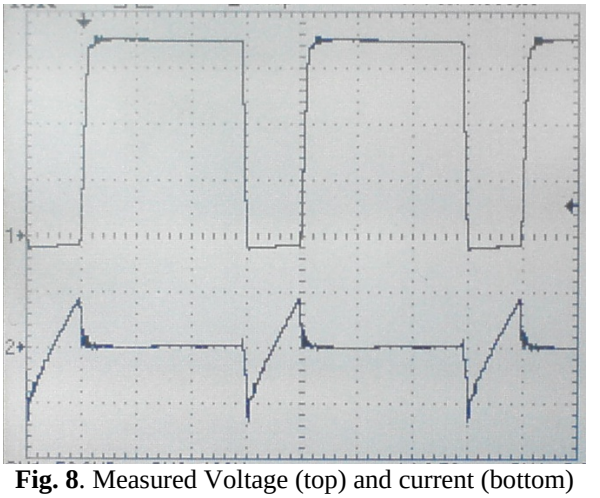

Fig. 8. Measured Voltage (top) and current (bottom) waveforms of the auxiliary switch (vertical scale 60V/div or 5A/div, time scale 2.5µs/div)

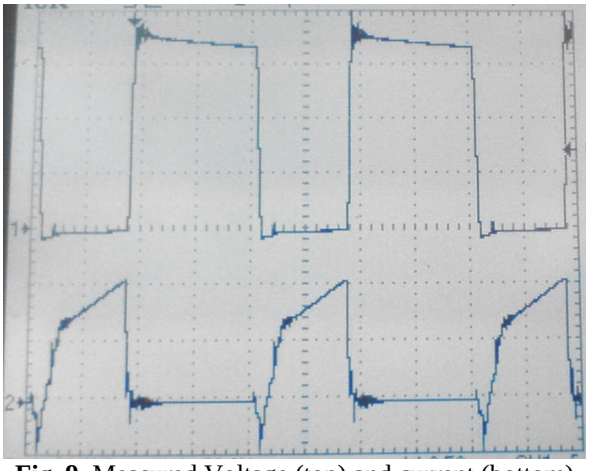

Fig. 9. Measured Voltage (top) and current (bottom) waveforms of the main Switch (vertical scale 30V/div or 3A/div, time scale 2.5µs/div)

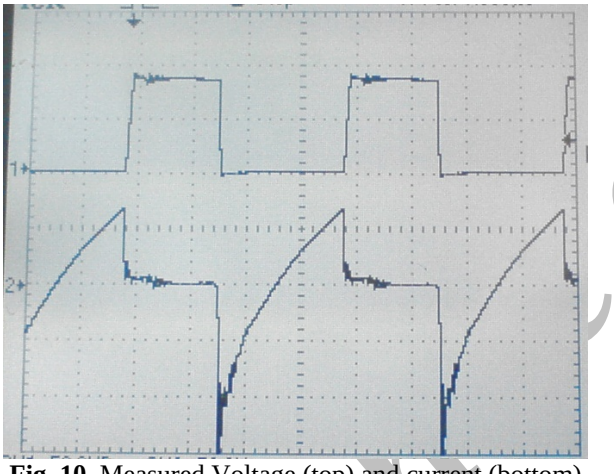

Fig. 10. Measured Voltage (top) and current (bottom) waveforms of the auxiliary switch (vertical scale 60V/div or 3A/div, time scale 2.5µs/div)

6. CONCLUSION

In this paper, a new soft switching isolated buck-boost PWM converter with active clamp circuit is proposed. The active clamp circuit in this converter not only absorbs voltage spikes across the main switch but also provides ZV condition for both main and auxiliary switches. Therefore this converter can operate under higher switching frequency to further reduce the converter size and weight. All switches are PWM controlled which simplifies the control implementation. The soft switching conditions exist in both buck and boost modes of converter operation over a wide input voltage range and can be employed in power factor correction. The experimental results of the implemented prototype circuit confirm the integrity of the proposed circuit.

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