

An Hybrid Multi Level Inverter Based DSTATCOM Control

K. Ramash Kumar¹, D. Kalyankumar², Dr. V. Kirubakaran³

1- AM.S.College of Engineering/Department of Electrical and Electronics Engineering, Chennai, India.

Email: ramash1210@yahoo.co.in (Corresponding author)

2- Saranathan College of Engineering / Department of Electrical and Electronics Engineering, Tamilnadu, India.

Email: kalyan_mtech_52@yahoo.co.in (Corresponding author)

3- Gandhigram Rural University / Department of Rural Energy, Tamilnadu, India.

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ABSTRACT:

This paper presents an investigation on the Hybrid Seven-Level (HSL) H-bridge inverter, which is used in a Distribution Static Compensator (DSTATCOM) in Power Systems (PS). Making use of HSLI has the benefits of low harmonics distortion, reduced number of switches required to achieve the seven-level inverter output over the conventional cascaded seven-level inverter, and also reduced switching losses. In order to compensate the reactive power and suppress the total harmonics distortion (THD) drawn from a Non-Liner Diode Rectifier Load (NLDRL) of DSTATCOM, we propose a Sub-Harmonics Pulse Width Modulation (SHPWM) technique to control the switches of HSL H – bridge inverter. The D-Q reference frame theory is used to generate the reference compensating currents for DSTATCOM and proportional and integral (PI) control is used for capacitors dc voltage regulation for DSTATCOM. An HSL H-bridge inverter is considered for the shunt compensation of a 4.5 kV distribution system. The results are validated by MatLab/Simulink simulation software.

KEYWORDS: DSTATCOM, Sub-Harmonic Pulse Width Modulation, Proportional-Integral Control, D-Q Reference Frame Theory.

1. INTRODUCTION

Shunt compensation for medium voltage distribution systems requires higher rating for voltage source converters (VSCs). Ratings of the semiconductor devices in a VSC are always limited; therefore, for higher rated converters it is desirable to distribute the stress among the number of devices using multilevel topology [1]. Cascaded multilevel configuration of the inverter has the advantage of its simplicity and modularity over the configurations of the diode-clamped and flying capacitor multilevel inverters. Application of cascaded multilevel converters for shunt compensation of distribution systems has been described in [2]-[3].

The multilevel power conversion has been receiving increasing attention in the past few years for high power application [4]. Numerous topologies have been introduced and studied extensively for utility and drive applications in the recent literature. These converters are suitable in high voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltage with a limited maximum device rating [1]-[4]. There are various current control methods for two-level converters [5]. Hysteresis control of power converters, based on instantaneous current errors, is

widely used for the compensation of the distribution system as it has good dynamic characteristics and robustness against parameter variations and load nonlinearities [6].

A DSTATCOM is a voltage source converter (VSC) based device. When operated in a current control mode, it can improve the quality of power by mitigating poor load power factor, eliminating harmonic content of load and balancing source currents for unbalanced loads [6]-[7].

Therefore, in this paper HSL H – bridge Inverter based DSTATCOM control in PS is proposed. A SHPWM technique is used as control for DSTATCOM. The HSL H – bridge inverter topology based DSTATCOM balances the source currents and reduces THD while improving the load power factor. The simulation of DSTATCOM with its control model is implemented in MatLab/Simulink. In section 2, we will present the operation of HSL H – bridge Inverter. The control of DSTATCOM is presented in section 3. A SHPWM technique is well executed in section 4. Simulation results of the system are discussed in section 5. The conclusions and future work of the system is discussed in section 6.

2. OPERATION OF HYBRID SEVEN LEVEL H - BRIDGE INVERTER

Normally, the voltage blocking capability of high speed devices such as Insulated Gate Bipolar Transistors (IGBT), and the switching speed of high voltage device like Integrated Gate Commutated Thyristors (IGCT) is found to be limited [8]. With a modular H-bridge topology [8], realization of multilevel inverters using a hybrid approach involving IGBTs and IGCTs operating in synergism is possible.

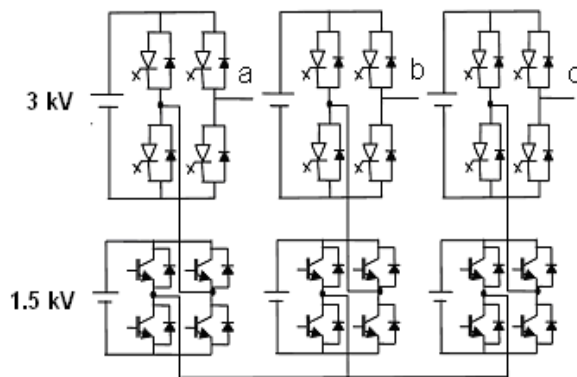


Fig. 1. Simplified schematic of the Hybrid Seven Level H- Bridge Inverter.

Table 1. Switching Between a and b of inverters

Command Signal (Desired Output)	GTO Inverter	IGBT Inverter
Between -4.5 and -3.0 kV	-3.0 kV	0 \leftrightarrow -1.5 kV
Between -3 and -1.5 kV	-3.0 kV	0 \leftrightarrow 1.5 kV
Between -1.5 and -0.0 kV	0.0 kV	0 \leftrightarrow -1.5 kV
Between 0.0 and 1.5 kV	0.0 kV	0 \leftrightarrow 1.5 kV
Between 1.5 and 3 kV	3 kV	0 \leftrightarrow -1.5 kV
Between 3 and 4.5 kV	3 kV	0 \leftrightarrow 1.5 kV

Hybrid multilevel inverter topologies have been studied for high power applications in [9-10]. The topology presented in reference [10] combines a Gate Turn-Off (GTO) thyristor based inverter, and an IGBT inverter, similar to that shown in Fig. 1. It may be verified that with a combination of 3 kV and 1.5 kV dc bus voltages in this topology, it is possible to synthesize stepped waveforms with seven voltage levels viz -3.5 kV, -3 kV, -1.5 kV, 0, 1.5 kV, 3 kV, 4.5 kV at the each phase leg output. As shown in Fig. 1, the higher voltage levels (± 3 kV) are synthesized using GTO inverters while lower voltage levels (± 1.5 kV) are synthesized using IGBT inverters. But it is well known that switching capability of GTO thyristors is limited at high frequencies [9]. Hence, a hybrid modulation strategy which incorporates stepped synthesis in conjunction with variable pulse width of the consecutive steps is proposed. The switching state

of the inverters for various levels of command signal is listed in Table 1.

3. DSTATCOM CONTROL

Fig. 2 shows a three-phase four-wire distribution system that is compensated by a DSTATCOM in PS. The three-phase load is supplied from the voltage source V_{sk} through the feeder with the impedance of (R_{sk}, L_{sk}) , where $k = a, b, c$ for the three-phase respectively. The DSTATCOM is represented by VSCs in the shunt path with the interfacing inductance L_{shk} . The resistance R_{shk} represents the loss equivalent due to the inverter switching. The voltage at the Point of Common Coupling (PCC) is denoted by V_{tk} . The currents flowing through the different branches at the PCC are the source current I_{sk} , the load current i_{lk} and the current injected in shunt branch I_{skk} .

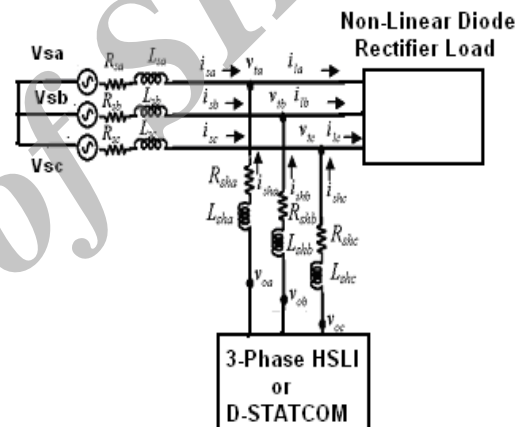


Fig. 2. Shunt compensation of three-phase DSTATCOM in PS.

3.1. Reference currents generation

There are several methods to extract the harmonic components from the detected three-phase waveforms [7]. Among them, the so-called p-q theory based on time domain has been widely applied to the harmonic extraction circuit of active filters. The detected three-phase voltage is transformed into the D-Q coordinates as shown in Fig. 3. The second order digital High Pass Filters (HPFs) with the same cut off frequency as 20Hz extract the dc component V_{hd}^* , V_{hq}^* , and V_0 which corresponds to the fundamental frequency in the coordinates.

In line – voltage regulation part is performed by a feedback control. Two co – ordinates V_d and V_q is compared with harmonic extracted voltage V_{hd}^* and V_{hq}^* . A gain K_v amplifies and to produce current references for harmonic damping I_{hd} , I_{hq} , and I_0 as shown in equation (1), equation (2), and equation (3). The current reference for the voltage – source inverter is the sum of the current references from the three parts, as follows:

$$I_{cd}^*(s) = K_v (G_h V_{hd}^* - V_d) + (V_{dc}^* - V_{dc}) \quad (1)$$

$$I_{cq}^*(s) = K_v (G_h V_{hq}^* - V_q) \quad (2)$$

$$I_0^*(s) = 1/3 (V_{sa} + V_{sb} + V_{sc}) \quad (3)$$

The obtained current reference is converted to three phase current reference by inverse D-Q transformation I_{ca}^* , I_{cb}^* , and I_{cc}^* . The three-phase reference compensating current is compared with the DSTATCOM compensating current extracted from ac system. Thus three phase compensating current I_{ca} , I_{cb} , and I_{cc} are produced.

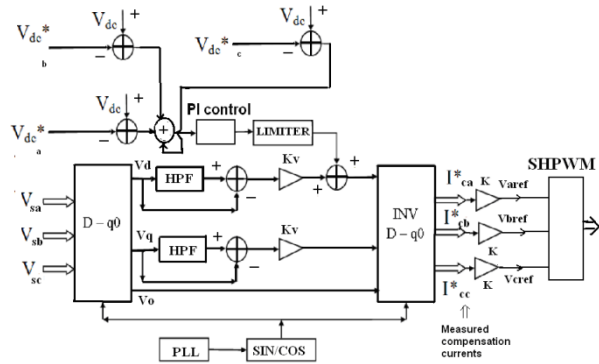


Fig.3. Block diagram of the control circuit equipped with the function of voltage regulation and harmonic damping or reduction.

Each phase of the compensating currents is amplified by a gain K in order to produce the three AC voltage references of the feedback loop, given by:

$$V_{aref} = K * (I_{ca}^* - I_{mca}) \quad (4)$$

$$V_{bref} = K * (I_{cb}^* - I_{mcb}) \quad (5)$$

$$V_{cref} = K * (I_{cc}^* - I_{mcc}) \quad (6)$$

Finally, each voltage reference of the DSTATCOM is compared with a multicarrier triangular waveform (1000 Hz) to generate the switching patterns for the HSL H – bridge Inverter.

3.2. DC bus voltage control

A DC bus controller is required to regulate the DC bus voltage V_{dc} , and to compensate the inverter losses in Fig. 3. The measured DC bus voltage V_{dc} of each phase is compared with its reference value V_{dc}^* . Similarly, the remaining phases are added all the error signals. The resulting error is applied to a PI regulator. The proportional and integral gains are set to $0.4 \Omega^{-1}$ and $2 \Omega^{-1} s^{-1}$, respectively [11]. Moreover, the DSTATCOM can build up and regulate the DC capacitor voltage. The electrical quantity to be controlled in the dc-voltage feedback loop is $(V_{dc}^* - V_{dc})$.

3.3. Sub-harmonics pulse width modulation technique

Conventional SHPWM technique for multilevel inverters employ extension of carrier based techniques for two level inverters. It has been reported that the spectral performance of a five level waveforms can be significantly improved by employing alternative dispositions and phase shift in the carrier signals [12]-[13]. This paper extends this concept to a seven level case, where the available options for polarity and phase variation. The carrier polarity variation is implemented control for DSTATCOM in this paper. It is based on a comparative evaluation of possible dispositions of triangular carrier waveforms depending on their relative polarities. For an m -level inverter this technique requires $m-1$, which are compared to a reference sine wave. Thus, for a seven-level inverter the number of carrier signals is six, and there exists five possible carrier signal configurations. The carriers are named $+3V$, $+2V$, $+1V$, $-1V$, $-2V$ and $-3V$ after their dc position. Their phase position is $+$ for a carrier in phase and $-$ for a carrier 180 degree out of phase as shown in Fig.5.

4. SIMULATION RESULTS

The main purpose of this section presents the simulation results of DSTATCOM in PS. Simulations have been performed on the DSTATCOM in PS with parameters listed in Table 2. The performance of system is evaluated in MatLab/Simulink. The THD in the source current for uncompensated system is 10.5%. The three-phase currents are unbalanced with the poor power factor. Fig. 4 shows the source currents for the uncompensated system. It is desired to bring down the THD in source current to be within an acceptable limit with good tracking of fundamental component while balancing the three-phase source currents.

Table 2. Parameters of DSTATCOM.

Parameters name	Numerical Value
Source voltage Vsk	4.5 kV , 50 Hz (line r.m.s)
DC Capacitors	5000 uF
D.C capacitor reference voltage (each phase)	4.5 kV
switching frequency	1kHz
Diode rectifier Non- linear Load resistance and inductance	20Ω , 0.1 mH
Shunt inductance and resistance	2mH, 0.1 oHm
Source resistsnce and inductance	1mH, 0.1 oHm

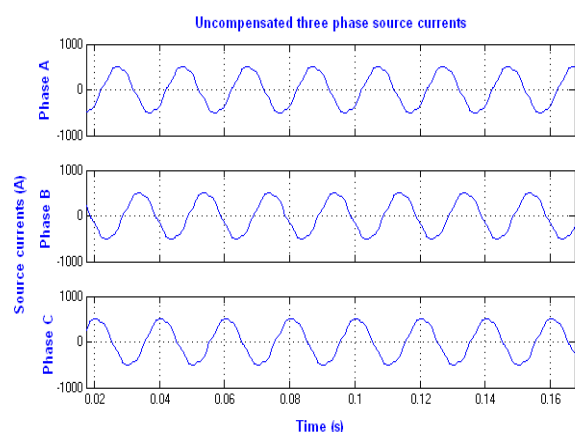


Fig. 4. Three phase source currents for uncompensated DSTATCOM in PS.

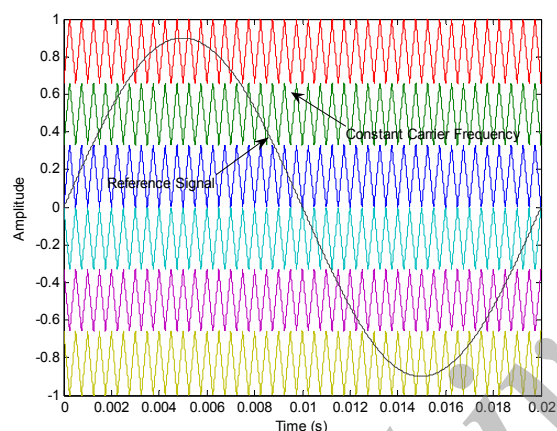


Fig. 5. Reference and carriers signals for SHPWM technique.

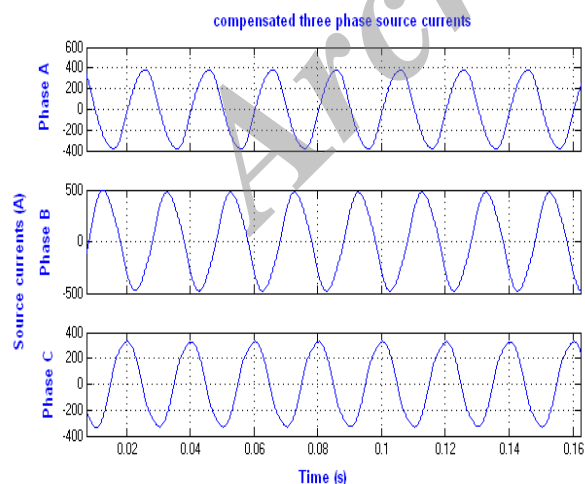


Fig. 6. Three phase source currents for compensated DSTATCOM in PS.

Fig. 5 shows generation of reference and carriers signal for SHPWM technique, which is used to control the switches of HSL H- bridges inverter.

Fig. 6 shows the compensated source currents using the proposed modulation and control. The source currents are balanced with the THD improved to 4.23% as shown in Fig. 7.

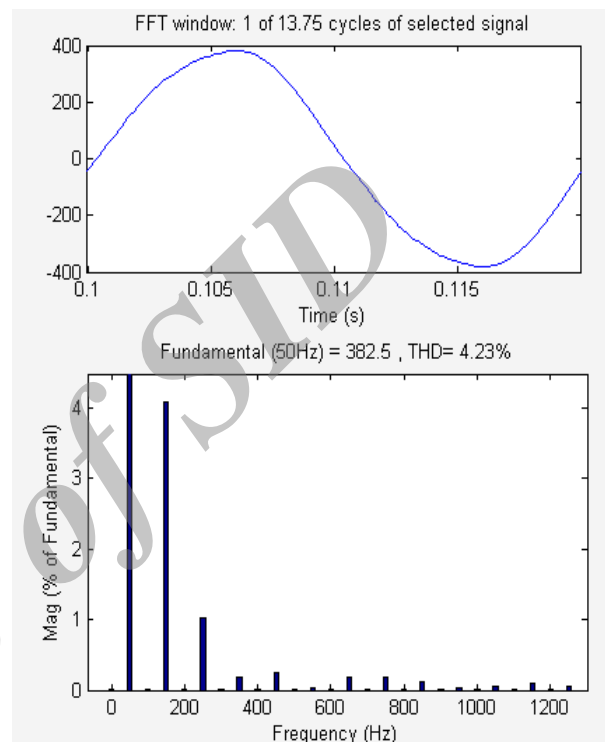


Fig. 7. THD for phase A source currents of compensated DSTATCOM in PS.

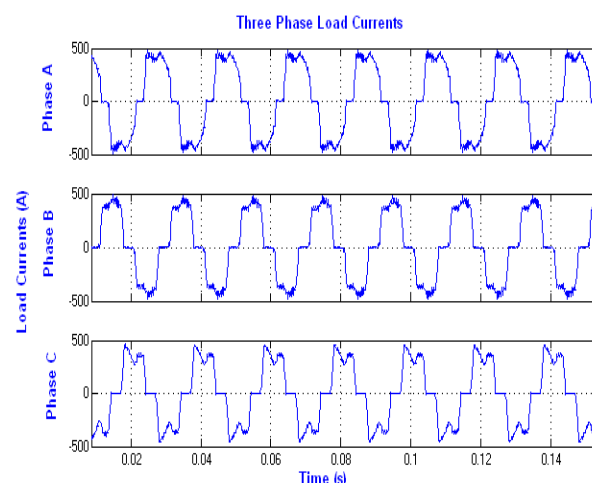


Fig. 8. Three phase load e currents for compensated DSTATCOM in PS

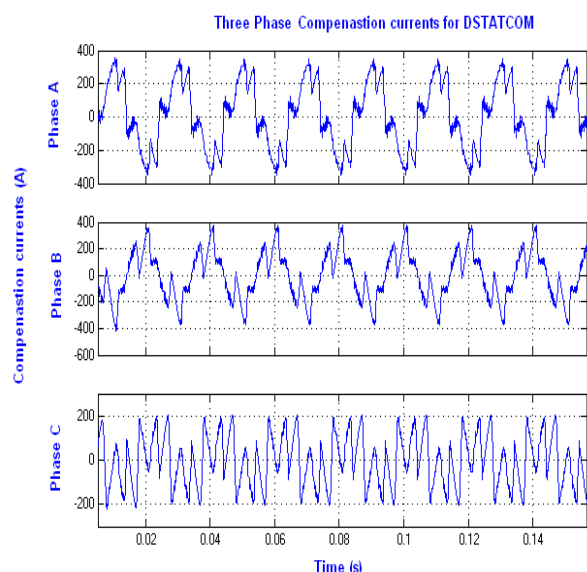


Fig. 9. shows the three phase compensated currents source currents for DSTATCOM.

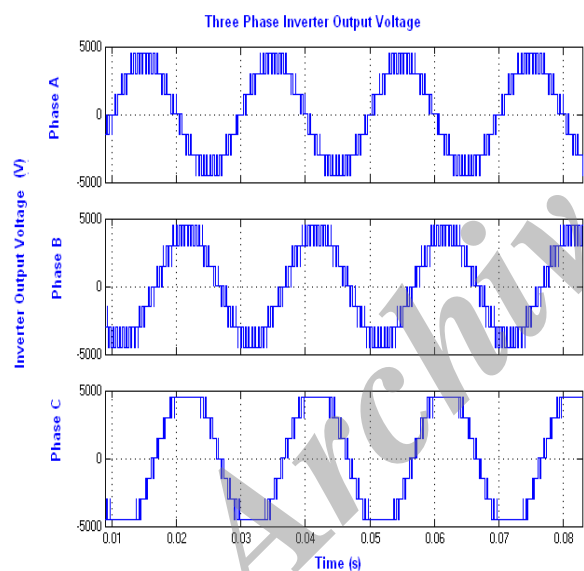


Fig. 10. Inverter output voltage for three phases.

Fig. 8 shows the load currents for the compensated system. The shunt current tracking characteristic is shown in Fig. 9. An error of about 25 A (rms) is observed in the tracking of the fundamental component.

The 7-level inverter output voltage for the phases-a, b and c is shown in Fig. 10. Fig. 11 shows the seven level inverter output voltage for a-phase. An average switching frequency of 1000 Hz is observed for all the switches. The source current is in phase with the terminal source voltage as shown in the Fig. 12 (for phase-a only). This implies a near unity power factor operation.

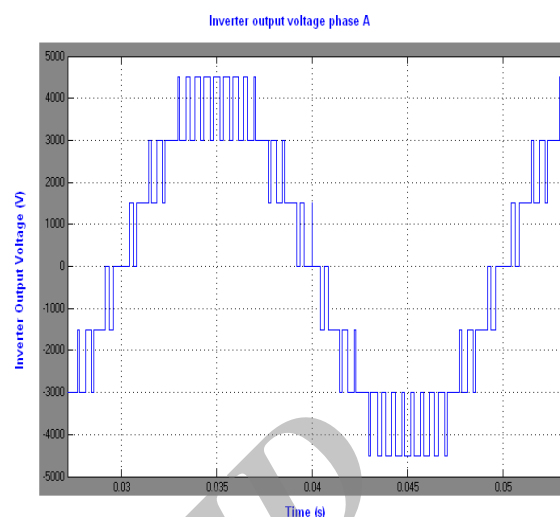


Fig. 11. Inverter output voltage for phase - a.

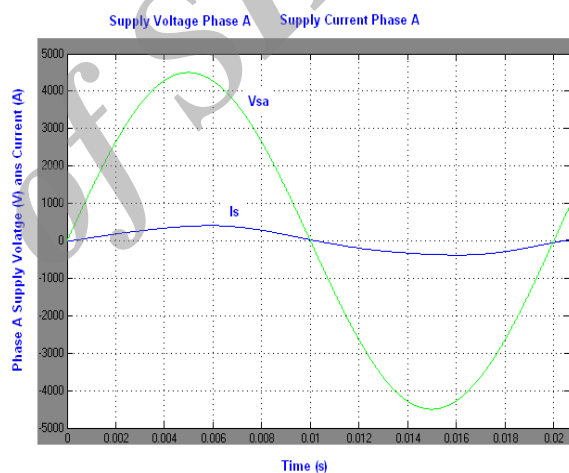


Fig. 12 In-phase source current with terminal voltage for phase-a.

Fig. 13 shows the convergence of the dc-link voltage of the cascaded HSL H – bridges Inverter for the phase-a. It can be found that the dc voltage has small ripple with designed PI control.

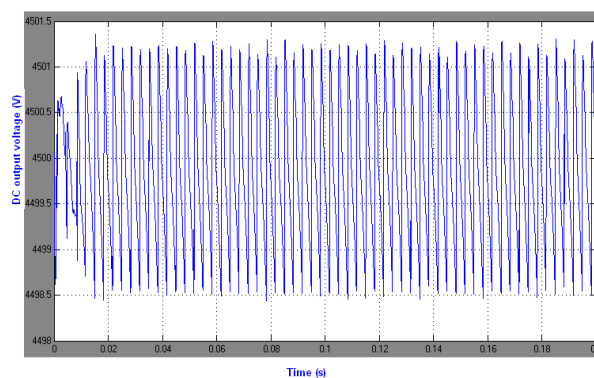


Fig. 13. DC link voltage convergence of the cascaded H-bridges for phase-a.

5. CONCLUSIONS

This paper studied a HSL H – bridge inverter used in a DSTATCOM in PS and has been successfully demonstrated in MatLab/Simulink. The benefits of HSL H – bridge inverter has low harmonics distortion, reduced number of switches to achieve the seven-level inverter output over the cascaded seven level inverter and reduced switching losses.

The HSL H – bridge inverter is studied for installation on a power distribution system, with the focus on harmonic reduction and voltage regulation performances. Harmonics present in the distribution system is significantly reduced by HSL H – bridge inverter. The results were showed good dc bus voltage – regulation, reduced source harmonic currents and have the stable operation. The further work focuses on the study of intelligent control for DSTATCOM.

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