Crosstalk Enhancement in 32 nm FD SOI MOSFET using HR Substrate and Multilayer BOX

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ABSTRACT:
In this paper, the crosstalk in 32 nm UTB SOI MOSFET is examined by using a new structure, a high resistivity substrate, and a multilayer BOX (SiO_2-Diamond). The electrical and thermal characteristics of the conventional SOI and a multilayer BOX SOI are compared, and it is concluded that parasitic capacitances and crosstalk are improved by incorporating multilayer BOX to a HR Substrate. In a conventional HR FD SOI, crosstalk is approximately -121dB, while by incorporating multilayer BOX substrate and increasing the thickness of the Diamond to 100nm, crosstalk can be reduced by 20%.

KEYWORD: Ultra Thin Body Silicon-on-Insulator MOSFET, Parasitic Capacitance, High Resistivity Substrate, Crosstalk, Diamond.

1. INTRUDUCTION

Due to the scaling of MOSFETs in the nanometer regime, Silicon-on-Insulator[1] MOSFET has become a promising technology for implementing over millions of transistor, in a single chip. The advantages of SOI MOSFET over BULK one in such a chip include: lower leakage current and noise, enhancement of short channel effect[2] and latch-up and also reduced parasitic capacitances [1]. The presence of buried oxide[3] in SOI MOSFET isolates the active region from the substrate, electrically. However, this BOX can lead to the self-heating effect[4] due to its lower thermal conduction over silicon layer [2].

By scaling MOSFETs, the obstacles such as the depletion region of the poly silicon gate and the high resistance of the gate rise. As a result, it is essential to decrease the thickness of gate oxide, while increasing the doping of channel for reduction of SCEs. The use of thin gate oxide and high doping for channel can lead to tunneling through gate oxide and reduction of mobility resulting in some limitations on scaling the device [3]. However, the ultra thin body[5] can reduce SCE, significantly. Furthermore, the undoped bodies ($10^{15}cm^{-3}$) can be useful for achieving the higher mobility's and drive current. In addition, the undoped bodies for reducing the threshold voltage variations due to the variation of statistical doping are applicable [3]. In these bodies, we have to use the engineering of work function to set the threshold voltage. In metal gates, the problem of the poly silicon gate (depletion region) is disappeared. Therefore, using metal gate in SOI MOSFET, the thickness of the gate oxide is reduced in comparison with the poly silicon gate with constant t_{OX}. The research resulting show t_{OX} reducing, improves the subthreshold slope and decreases drain induced barrier lowering[6] [3]. Then, in this device, a metal gate was used.

One of the main problems that SOI MOSFETs present when integrated as a single chip for RF application is the transmission of signal between adjacent MOSFETs through their substrates (known as crosstalk effect) [4]. There have been a lot of efforts such as using low resistivity[7] substrate, in order to improve the crosstalk effects, but any of them has faced some challenges. Using LR substrate (the resistance of substrate is considerably less than that of load (50Ω)) leads to the rise of parasitic capacitances [4]. It is advisable to use the HR substrates. However, the HR substrates can result in the increase of crosstalk effects [5]. In order to reduce the crosstalk effect in HR substrates, the different solutions like increasing the density of traps at the interface of BOX-substrate have been applied to the structures, but they make the fabrication of devices more difficult [5].

In this paper, we have to use the HR substrate and in order to reduce parasitic effects, a new structure of

fully depleted SOI[8] MOSFET with multilayer BOX is introduced. Then, by analyzing and comparing the electrical and thermal characteristics of both new and conventional MOSFETs, it is concluded that parasitic capacitances and crosstalk improve in new MOSFET. The use of diamond in BOX decreases crosstalk effects around 20%. This diamond layer not only improves some characteristics such as, SHE, drive current and parasitic capacitances, but also has no negative effect on other ones.

2. DESIGN AND SIMULATION OF HR UTB SOI WITH 32NM CHANNEL LENGTH

2.1. Design

Cross sections of conventional and new n-channel SOI MOSFET (designed, in order to increase the crosstalk immunity), are shown in Fig. 1 (a) and (b), respectively.

The active region between source and drain is called channel. T_{Si}, t_{OX} and T_{BOX} are silicon film, front gate and back gate thicknesses, respectively. These transistors consist of four terminals namely source, drain, front gate and back gate (substrate).

The operation regions of SOI MOSFET depend on both thickness and doping of silicon film. SOI MOSFETs are divided to: fully depleted SOI and partially depleted SOI[9]. In PD SOI, the thickness of silicon film is bigger than maximum depletion width ($T_{Si}>X_{dmax}$). So, the silicon layer isn't depleted completely. In FD SOI MOSFETs, the thickness of silicon film is smaller than maximum depletion width ($T_{Si}<X_{dmax}$) and which is why the silicon layer is depleted entirely. As a result, by applying the threshold voltage to the front gate of FD SOI, the silicon film is depleted completely neglecting back-gate bias [6].

2.2. Simulation setup

Ultra thin body SOI MOSFET showing improvement such as reduced SCE and lower junction leakage current over other MOSFETs is analyzed in this paper [6]. Due to the reduction of silicon film thickness, the parasitic capacitances are reduced and as a result, crosstalk immunity increases. The thermal diffusion ability decreases in source and drain regions. Then the ultra thin body raises after that the self-heating effects increases very much. Therefore, the parameters such as mobility and drive current are affected and reduced [2].

In this paper, by using ISE-TCAD simulator, the output characteristics of a 32nm FD SOI is achieved, and The Hydrodynamic model is used for simulations [7]. Using this model (specified for scaled MOSFET in, nanometer regime), accurate characteristic of temperature in MOSFET is achieved. In the hydrodynamic model, the energy conservation equations for electrons, holes and the lattice are solved. In this model, despite drift-diffusion model, the carrier temperatures T_n and T_P are not equal the lattice temperature T_L [7].

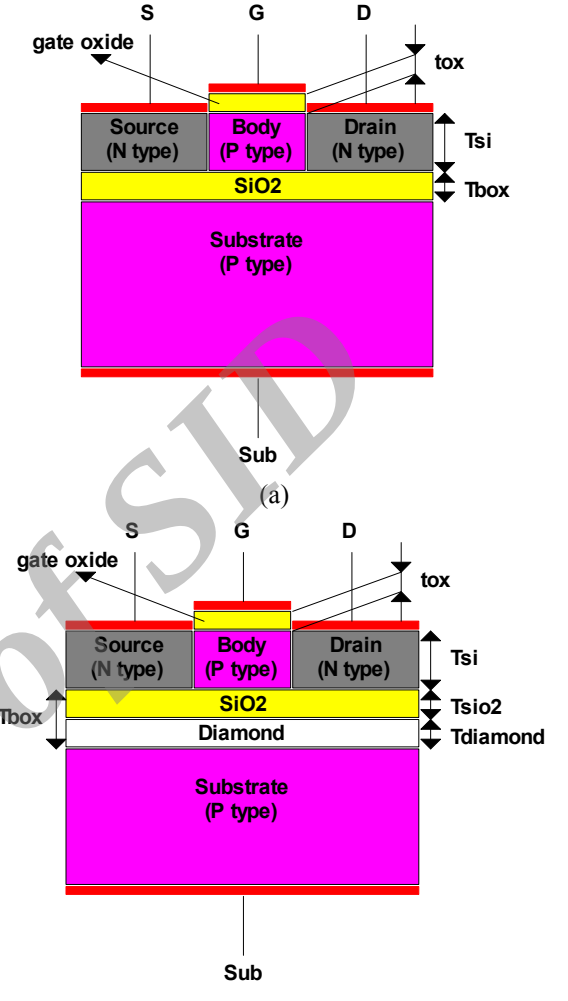

Fig. 1. Cross section of n-channel (a) conventional MOSFET (b) new MOSFET with multilayer BOX (SiO_2 and diamond).

The details of the device parameters investigated here are given in Table1.

Table 1. Device parameters chosen in the simulation

Physical gate length(L_G)	32 (nm)
Gate oxide thickness(t_{OX})	1 (nm)
SiO_2 thickness(T_{Sio2})	30 (nm)
Diamond thickness($T_{diamond}$)	10,40,80,100 (nm)
Silicon film thickness(T_{Si})	5 (nm)
Substrate doping	1×10^{15} , 3.5×10^{12} (cm^{-3})

In order to comply with ITRS[10] requirements in terms of designing FD SOI MOSFET, film thickness should follow the equations defined as [6]:

$$T_{Si} \le \frac{1}{4} L_G \quad (1)$$

$$T_{Si} < X_{d\max} \quad (2)$$

L_G and X_{dmax} are channel length and maximum depletion width, respectively. So, in UTB SOI (investigated in this paper), the thickness of silicon film should be equal to 5nm.

For simulations, two devices with standard[11] and high resistivity[12] substrate are used. For standard substrates, doping of substrate (N_{SUB}) is $1\times10^{15}cm^{-3}$. The resistance of HR substrate is considered to be 1KΩ. So, according to the equation 3, the doping of substrate is computed [8].

$$N_{SUB} = \frac{1}{q\rho\mu} \quad (3)$$

In equation 3, q is the charge of electron and is equal to 1.6×10^{-19}c, μ indicates the mobility of majority carriers and N_{SUB} is the doping of substrate.

DIBL is one of the short channel effects occurring in UTB SOI, and reflects the electrostatic influence of a drain voltage (V_D) on the source-channel barrier height. As V_D is increased, the source-channel barrier height is reduced leading to an increased injection of source majority carriers in the channel, hence V_T decreases with V_D, which exponentially increases the leakage current [2]. When BOX thickness (only SiO_2) is 30nm, DIBL is 63mV/V.

Subthershold swing is one of the subthreshold characteristics which indicate how effectively the transistor can be turned off when V_{gs} is decreased below V_{TH}. For UTB SOI, SS is given by [2]:

$$SS = 2.3\frac{KT}{q}\left(1+\frac{C_{BOX}}{C_{OX}}\right) \quad (4)$$

In that C_{BOX} and C_{OX} are the capacitances of the BOX and front gate dielectric, respectively. Drain voltage is taken 0.05V in the SS simulation. For the device with 30nm BOX thickness (only SiO_2), SS is 67mV/decade.

The transconductance of a MOSFET, g_m, is a measure of the effectiveness of the control of the drain current by the gate voltage. The transconductance of a FD SOI MOSFET can be obtained from equation 7 [1].

$$g_m = dI_{Dsat}/dV_G \quad (5)$$

3. RESULTS OF SIMULATION

Over last years, the high resistivity substrates have been known as a solution for integrating the MOSFETs for RF applications [5]. The values of C_{BOX} and C_{DS} versus the BOX thickness in an UTB SOI with standard and high resistivity substrates are presented in Fig. 2.

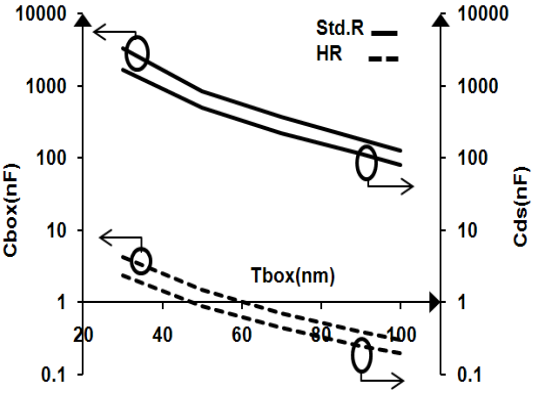

Fig. 2. C_{BOX} and C_{DS} as a function of BOX thickness in UTB SOI with different substrates; standard resistance (Std.R) and high resistance (HR).

In UTB SOI with the high resistivity substrate, due to the presence of fixed charges in BOX layer, a weak inversion layer is made at the BOX-substrate interface. As a result, there is a significant reduction in parasitic capacitances (Fig. 2) [8]. Moreover, regarding the relation $C_{BOX}=\varepsilon_{BOX}/T_{BOX}$ (T_{BOX} and ε_{BOX} are the thickness and dielectric constant of BOX, respectively.) the thicker the BOX thickness is, less the capacitances become.

Having discussed the advantages of high resistivity substrates, they have replaced the standard ones for designing the RF circuits. The weak inversion layer at SiO_2-high resistivity substrate interface causes a shallow conduction layer at the interface, resulting in the reduction of the effective resistance over this area [5]. One of the obstacles in SOI structures for RF application is the crosstalk effect.

First, in order to analyze the influence of substrate on crosstalk, an equivalent circuit, shown in Fig. 3, is presented for modeling the silicon substrate [5].

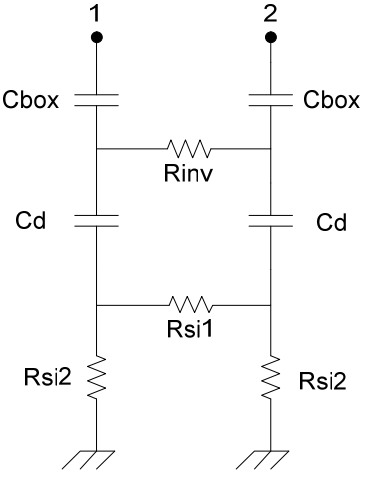

Fig. 3. Equivalent lumped element circuit for silicon substrate

This model consists of two points (1, 2) for receiving and transmitting signals. C_{BOX} is the capacitance of BOX and R_{inv}, which is small despite using high resistivity substrate, shows the resistance of parasitic conduction layer at the BOX-substrate interface [5].

On data from Fig. 3, the BOX capacitance is located in the way of signal transmission from point 1 to point 2. Therefore, the rise of capacitance impedance results in the reduction of signal transmission [4]. In addition, when the higher drain voltage is needed for making a weak inversion layer at the interface of BOX-substrate, the low resistance of this parasitic conduction layer (R_{inv}) is developed slower, and as a result, crosstalk is reduced.

In order to measure the crosstalk, the two same MOSFETs are connected to each other and the S_{21} parameter (S parameter between drain1 and drain2) is calculated. In ISE-TCAD software, the S parameters are extracted from Y parameters, considering equation 6:

$$S = (Y_0.I + Y)^{-1}(Y_0.I - Y) \quad (6)$$

Y, S and Y_0 (= 1/ Z_0, Z_0 is the characteristic impedance equal to 50Ω) are the matrixes of admittance, scattering and characteristic admittance, respectively.

In Fig. 4, the crosstalk effect (as a function of frequency) in HR substrate is indicated. As presented in Fig. 2, in the simulated device, using HR substrate, the BOX capacitance is reduced significantly in comparison with the standard substrate. Therefore, the BOX impedance rises, and it should result in the enhancement of crosstalk in the HR substrate MOSFET.

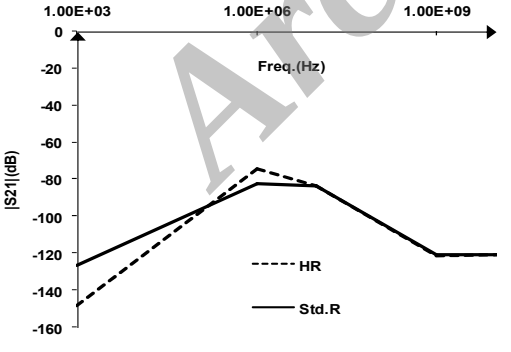

Fig. 4. Crosstalk in Std.R and HR substrates as a function of frequency.

Regarding Fig. 4, in lower frequencies, crosstalk in HR substrate improves over that in Std.R substrate, but by the increase of frequency, the effect of crosstalk in Std.R is reduced more than HR to the point that crosstalk in HR overtakes that in Std.R in some frequency. Over the higher frequencies, the crosstalk in both becomes the same. For this reason, there is no enhancement of crosstalk in HR substrate that this is due to the reduction of resistance at the interface of BOX-substrate [5].

Furthermore, the impedance of capacitance is reduced by the increase of frequency, and as a result, the crosstalk rises over higher frequencies [4].

In this paper, the aim is presenting a way, with which crosstalk is reduced by the improvement in R_{inv} in HR substrate. For this, a layer of diamond is put between SiO_2 and substrate. The presence of diamond layer causes the inversion layer to be made by higher voltages. Therefore, the resistance at the interface of BOX-substrate rises, and as a result, the input current to the second substrate through the first one is reduced, and crosstalk improves. The crosstalk in HR substrate with the multilayer BOX as a function of the thickness of diamond is shown in Fig. 5. As presented clearly from in Fig. 5, when there is no appearance of diamond (thickness=0), the crosstalk is equal to -121dB, and by the use of diamond layer and increase of its thickness to about 100nm, the crosstalk becomes equal to -145dB.

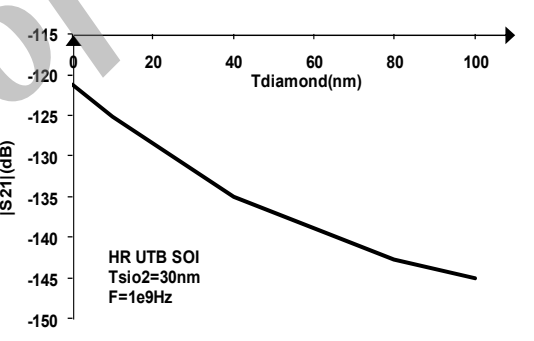

Fig. 5. Crosstalk as a function of diamond thickness at the frequency of 1 GHz.

In fact, by applying diamond layer between SiO_2 and substrate, the resistances at BOX-substrate interface rises. As a result, the input current into the second substrate through the first one decreases ending in crosstalk enhancement. By applying diamond layer in BOX, not only crosstalk improves, but also other parameters can be enhanced.

In a device with multilayer BOX, the BOX is made of two layers, namely SiO_2 and diamond (equation 7).

$$T_{BOX} = T_{SiO2} + T_{Diamond} \quad (7)$$

The thermal conduction of diamond is several times bigger than that of SiO_2. So, it is expected that SHE improves in multilayer BOX [9]. Fig. 6 shows the distribution of lattice temperature for two HR UTB SOI devices, one with SiO_2 BOX and another with SiO_2-diamond BOX. Analysis has been carried out for the position, X, along the channel. The thickness of SiO_2 in

both devices is the same (30nm). Furthermore, the temperature of substrate is set to 300K.

By growing the BOX thickness, the lattice temperature is expected to rise. However, in multilayer BOX SOI MOSFET, due to the increase of BOX thickness by using diamond and having higher thermal conduction over SiO_2, the lattice temperature doesn't increase significantly in comparison with thin BOX layer, in which only SiO_2 is used.

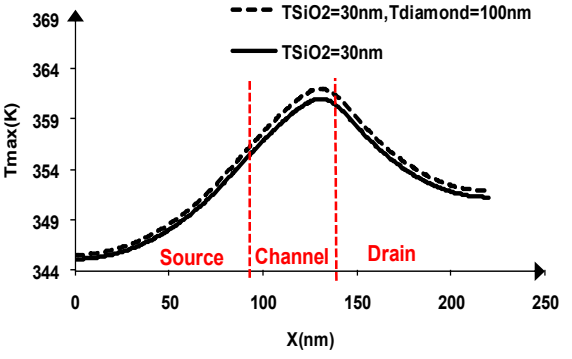

Fig. 6. Thermal profile along the channel (X) for two HR FD SOI MOSFETs.

Therefore, by enhancement of SHE in multilayer BOX device (SiO_2-diamond), the mobility and drive current improve. Fig. 7 presents the characteristics of drain current versus drain voltage in two various MOSFETs with 32nm channel length. The BOX of first MOSFET is composed of only SiO_2, while that of second one is made of SiO_2 and diamond.

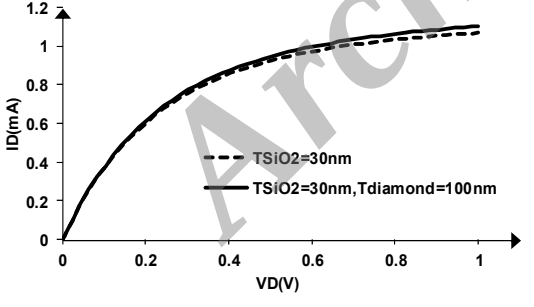

Fig. 7. I-V characteristics for two 32nm FD MOSFET

On data from Fig. 7, the output current of MOSFET with multilayer BOX is more than that of single layer BOX. The improvement in C_{DS} and C_{BOX} by using multilayer BOX is clearly shown in Fig. 8.

The BOX capacitance is the sum of SiO_2 and diamond capacitances. The use of diamond layer decreases the BOX capacitance.

Furthermore, the diamond layer in BOX doesn't present any negative effect on other parameters like transconductance, output conductance and subthreshold slope.

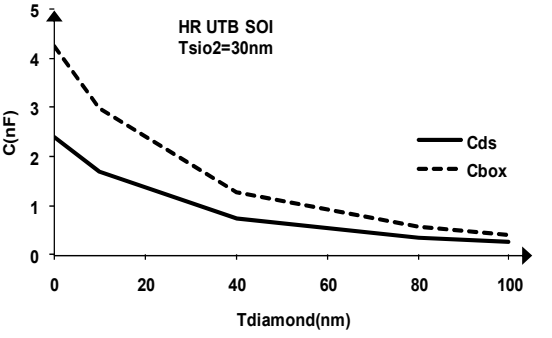

Fig. 8. C_{BOX} and C_{DS} as a function of diamond thickness for high resistivity silicon substrate.

4- CONCLUSION:

The parasitic capacitance and crosstalk in conventional SOI MOSFETs with the high resistivity substrate and standard substrate are analyzed, and it is shown that by using HR substrate, there is a significant reduction in parasitic capacitances. In order to improve crosstalk in HR substrate devices, a diamond layer is placed between SiO_2 and substrate, and it is indicated that diamond layer not only enhances SHE parasitic capacitances and drives current, but also has no negative effect on output characteristics of the device. Furthermore, the crosstalk is improvement. In HR 32 nm FD SOI MOSFET with single layer BOX (30nm), crosstalk is -121dB, but by incorporating multi layer box, and the increase of its thickness to 100nm, crosstalk is reduced by 20%.

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[1] - SOI
[2] - SCE
[3] - BOX
[4] - SHE
[5] - UTB
[6] - DIBL
[7] - LR
[8] - FD SOI
[9] - PD SOI
[10] - International Technology Roadmap for Semiconductors
[11] - Std.R
[12] - HR