*Journal of Technical Engineering Islamic Azad University-Mashhad Branch*

# A CMOS Ring Oscillator VCO with Quadrature Outputs and High-Tuning Range

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**Abstract** This paper presents the design of a new four-stage ring oscillator with quadrature outputs using a 0.13µm CMOS 1P8M technology. The oscillator utilizes feed-forward technique and negative resistance to reduce the delay per stage and provides high frequencies. Employing single PMOS transistor to vary the load impedance allows reaching ultra-wide tuning range. The output frequency ranges from 0.8 to 11.3 GHz, which is equivalent to nearly 175% tuning range, while the circuit consumes only 10mW. Simulation results illustrate a phase noise of -83dBc/Hz @ 1MHz offset from centre frequency. Also, the worst case phase variation due to mismatch is better than 0.4˚over the above frequency range.

**Keywords** CMOS ring oscillator, VCO, High tuning range, Phase noise, Quadrature Output.

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## 1.Introduction

VCOs are one of the important blocks of data communication systems and have wide applications, from data modulating in transmitters to demodulation and clock recovery in receivers. Ring inverter-based oscillators have some advantages among the other oscillators that have made them a good choice for designers [1]. Compared to other alternatives, particularly the LC resonator-based oscillators, the ring oscillator is compact and it can provide higher frequencies [2]. Further, its tuning range can span orders of magnitude as the ring oscillator is tuned by current. However, ring oscillators have some drawbacks, mainly lower Q factor and consequently larger phase noise.

An oscillator with broad-band tuning range can greatly reduce circuit complexity in currently wide-bandwidth communication systems. Meanwhile, it is desirable to scale down the current consumption of the VCO with frequency, as is interestingly possible in ring oscillators.

Ring oscillators with differential delay stages exhibit greater immunity to supply disturbance and substrate induced noise than single delay stage ones. However, single-ended ring oscillators can reach higher frequency with lower phase noise and power consumption compared to differential ring oscillators. Besides the tuning range and power consumption issues, quadrature outputs is becoming important for image rejection receivers, half rate clock recoveries, and multi-phase processor clocks [5].

In recent years, several novel cells have been proposed to reduce the delay of each cell. In [10] a source capacitively coupled current amplifier is adopted. In [5] a new technique to achieve quadrature outputs is proposed. Nevertheless, achieving low-power consumption, high frequency with wide tuning range, and low phase error and phase noise is a challenging task.

In this paper, a novel four-stage CMOS ring oscillator with quadrature outputs and negative resistance at the load is proposed, resulting in relatively higher frequencies and wider tuning range with low phase error.

The remainder of this paper is organized as follows. In section II, the structure of proposed ring oscillator is introduced. In section III, phase noise analysis is reported. Simulation results and comparison with other ring oscillators are presented in section IV. Finally, conclusion is given in section V.

## 2. Proposed ring oscillator

There are some known techniques to generate quadrature signals, but most are frequency dependent and cannot be used for high tuning ranges. Unfortunately, to produce quadrature outputs a ring needs even number of stages which has a stable operating point and does not oscillate. One technique to overcome this problem is to cross connect the output of one stage to the

input of the other stage. The other technique, as mainly addressed in this paper, is to add feed-forward inverters between nodes with opposite phases. Employing this technique not only allows generating quadrature signals, but also alleviates oscillating at higher frequencies by reducing the delay per stage.

**Feed-forward technique**

The frequency of a conventional single-loop ring oscillator is limited by the smallest delay provided by basic inverter delay cell. Hence various techniques have been explored to reduce the smallest achievable delay per stage, one of which is the feed-forward or dual-delay paths technique [5, 6]. In [6], a technique to increase the operating frequency of ring oscillators with an odd number of delay cells by creating feed-forward paths is presented. The concept and block diagram of a four-stage ring oscillator utilizing feed-forward technique is illustrated in Figure (1).

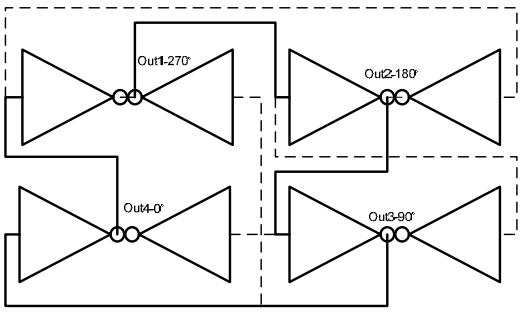


Figure 1 Block diagram of the proposed ring oscillator employing feed-forward scheme. Each stage is composed of two inverters

The basic concept of feed-forward technique is to add an additional path to the loop to avoid latch-up in even number rings and to increase the switching speed of each cell. The bold lines seen in Figure (1) represent the primary loop and the dashed lines represent the secondary loop. Secondary loops are added between the nodes with opposite phases and help the ring to oscillate in higher frequencies.

In contrast to a ring with an odd number of inverters, now two transitions are travelling through the ring. Therefore, the oscillation frequency is given by

$$f_{OSC} = \frac{1}{\tau_{Chain}} = \frac{1}{N\tau_{DelayCell}} \qquad (1)$$

**Proposed Delay Cell**

Figure (2) shows the schematic diagram of two delay stages with opposite phases. Each one is composed of two distinct inverters whose outputs are connected. The NMOS transistor M1 creates the input stage for primary loop, while the NMOS transistor M2 is the input transistor for secondary loop. M4 and M5 are utilized to control the frequency of operation by varying their gate-source voltage. Applying control voltage to PMOS transistors helps avoiding the tail current control mode, and consequently increasing output voltage swing while reducing 1/f noise. Furthermore, single control voltage relaxes the implementation of charge pumps and loop filters in the PLLs

[6]. The size of M4 and M5 determines the tuning range. Transistors M5 and M6 create load with negative impedance to reduce the delay of each cell. Instead of utilizing a conventional CMOS inverter cell as a delay stage, the PMOS transistors of both stages are replaced with single PMOS transistor in a positive feedback structure. This replacement enhances ring oscillator performance in three ways compared to a cell by conventional CMOS inverter: firstly, it reduces the overall capacitance of each cell and consequently improves the oscillation frequency. Secondly, adding negative resistance between two cells allows reaching higher frequencies. Thirdly, the oscillator will experience better phase error performance between the output signals as this feedback is employed.

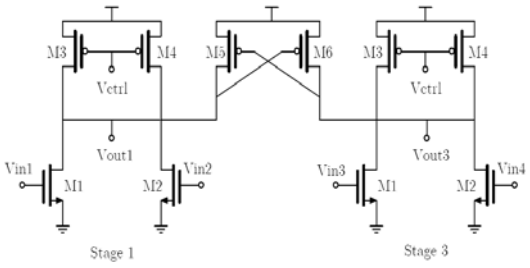


Figure 2 Two delay stages which are connected together with positive feedback showing negative impedance

Two PMOS transistors M5 and M6 create negative resistance. Considering the structure shown in Figure (3), and by neglecting drain-source conductance, we have:

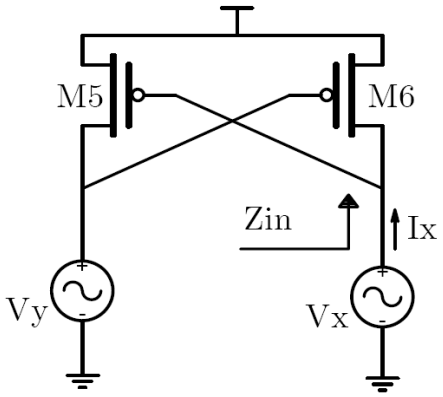


Figure 3 Negative resistance utilized between two delay cells

$$I_x = i_{ds} = -g_{m6}(-V_y) \quad (2)$$

$$V_x = -V_y \quad (3)$$

And

$$I_x = -g_{m6}V_x \rightarrow \frac{V_x}{I_x} = -\frac{1}{g_{m6}} \quad (4)$$

Therefore, the impedance at the drain of M6 is always negative and its magnitude can be changed by varying the widths of M5 and M6.

### 3. Calculation of Phase Noise in Proposed Oscillator

In order to have insight about noise mechanisms in proposed ring oscillator, Hajimiri's model is employed. As shown in [3], if the symmetry criteria is met to

minimize $\Gamma_{dc}$ and hence up-conversion of 1/f noise, the phase noise of the oscillator is dominated by white noise. For CMOS transistor, the drain current noise spectral density is given by

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_{d0} = 4kT\left(\frac{\gamma}{\alpha}\right)g_m \qquad (5)$$

where $g_{d0}$ is the zero-bias drain source conductance, $g_m$ is the device transconductance, the coefficient $\gamma$ is the MOSFET noise parameter. This coefficient is 2/3 for long channel devices in the saturation region and typically two or three times greater for short channel devices [4] and $\alpha = g_m / g_{do}$ .

**Proposed CMOS Ring Oscillator**

According to [3] the single-side band phase noise spectrum due to white noise current source is given by

$$L\{\Delta f\} = \frac{\Gamma_{rms}^2}{8\pi^2 \Delta f^2} \cdot \frac{\overline{i_n^2}/\Delta f}{q_{max}^2} \qquad (6)$$

where $\Gamma_{rms}$ is the rms value of the ISF function, $\overline{i_n^2}/\Delta f$ is the single sideband power spectral density of the noise current source, and $\Delta f$ is the frequency offset from the carrier.

Figure (4) shows typical waveforms of ring oscillator and impulse sensitivity function. The ISF is the function of output waveform and it accounts for the time-variant sensitivity of the oscillator to its noise sources. A high sensitivity to noise at the transitions of the output signals can be seen.

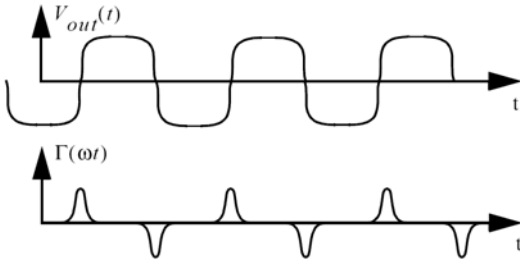


Figure 4 Typical waveforms of ring oscillator, including output signal and impulse sensitivity function of the oscillator

The approximate expression for $\Gamma_{rms}$ is [3].

$$\Gamma_{rms} = \sqrt{\frac{2\pi^2}{3\eta^3}} \frac{1}{N^{1.5}} \qquad (7)$$

where $\eta$ is proportionality constant and N is the number of stages.

Total output current noise of the delay cell should be calculated next. Considering the delay cell shown in Figure (2) M1, M2, M3, M4 and M5 noise source sum with each other resulting in the following expression:

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\,\gamma/\alpha\,(g_{m1} + g_{m2} + g_{m3} + g_{m4} + g_{m5)} \left(r_{01} \| r_{02} \| r_{03} \| r_{04} \| (-1/g_{m5})\right)^2 \qquad (8)$$

By considering that during a period

each node in the ring is charged to $q_{max}$ and discharged to zero, in an N-stage single-ended ring oscillator, the power dissipation associated with this process is $Nq_{max}V_{DD}f_0$. However, during the transitions, some extra current, known as crowbar current, is drawn from the supply. Consequently, the total power consumption is approximately given by [3]:

$$P = 2\eta N V_{DD} q_{max} f_0 \qquad (9)$$

By taking into account equations (6), (7) and (9), the final expression for the phase noise due to white noise can be determined by:

$$L\{\Delta f\} = \frac{f_0^2}{\Delta f^2} \cdot \frac{V_{DD}^2}{3\eta N P^2} \cdot \overline{i_n^2} / \Delta f \qquad (10)$$

Also, the total noise of each stage can be computed by (8).

On the other hand, flicker noise also contributes to the phase noise of the oscillator in the $1/f^3$ region by:

$$f_{1/f^3} = f_{1/f} \cdot \frac{\Gamma_{dc}^2}{\Gamma_{rms}^2} \qquad (11)$$

where $\Gamma_{dc}$ is the DC value of the $\Gamma(x)$ function. The up-conversion of device 1/f noise occurs through the $\Gamma_{dc}$ function.

## 4. Simulation Results and Performance Comparison

The proposed ring oscillator is simulated in a 0.13µm CMOS 1P8M technology. The width of M5 and M6 is set to minimum feature size to have the most negative impedance. The widths of main NMOS transistors (M1&M2) are set to minimize the capacitive effects while drawing allowable current for higher frequencies. The widths of M3 & M4 determine the frequency tuning-range.

Figure (5) illustrates the tuning characteristics of proposed VCO. By changing the control voltage between 0-0.8V, the frequency changes between 0.8-11.3 GHz (i.e., 175% tuning range). It shows linear characteristics and wide tuning range. This wide tuning range is the result of current controlling (or changing the load resistance of) the VCO by only a PMOS transistor and also the feed-forward and cross-coupled load which allows us to reach high oscillation frequencies.

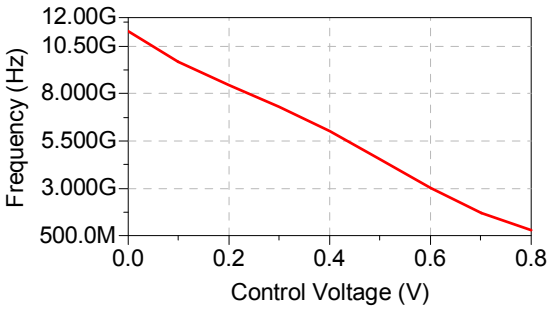


Figure 5 Frequency sweep with control voltage in proposed quadrature VCO

The circuit draws only 12mA and 0.45mA from 1.2V supply when running at highest and lowest frequency, respectively. This low-power consumption is achieved by utilizing single-ended structure and

consequently avoiding tail current, besides using feed-forward technique which results in reducing the time in which both NMOS and PMOS transistors are on.

The phase noise is calculated using Advanced Design System (ADS) harmonic balance simulation. It shows a phase noise of -83dBc/Hz@1MHz offset from center frequency. Figure (6) shows the simulation results.

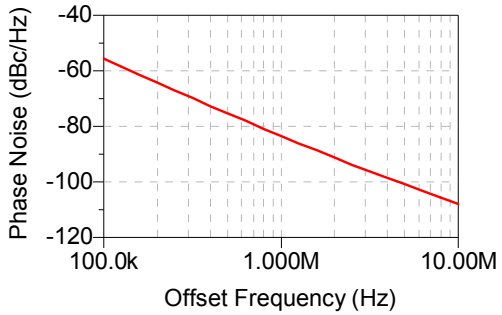


Figure 6 Phase noise simulation of proposed quadrature ring oscillator

Employing worst case mismatches between all transistors in the ring oscillator shows that phase variation in each quadrature output is better than 0.4˚ over 0.8 to 11.3 GHz frequency range. Figure (7) shows the phase variations over operating frequency (control voltage). Maximum phase error is only 0.6˚ at 11.3 GHz. Time domain quadrature outputs of the VCO are shown in Figure (8).

Figure (9) shows the oscillation frequency with process variations. Four corner cases are simulated which shows acceptable deviation from the typical condition shown in Figure (5).

The oscillation frequency variations with respect to temperature are illustrated in Figure (10) Slight changes occur over the temperature range 0-80° C.

Some other reported ring oscillators data are listed in Table (1) for performance comparison. The VCO performance may also be evaluated using the following figure of merit (FOM) equation:

$$FOM = -L\{\Delta f\} + 20\log(f_0/\Delta f) + 10\log(T.R.) - 10\log(P_{dc}/1mw) \quad (12)$$

where $L\{\Delta f\}$ is the phase noise at $\Delta f$ offset frequency from center frequency $f_0$, T.R. is the tuning range from center frequency $f_0$ (%), and $P_{dc}$ is the power consumption in mW.

Clearly, the proposed quadrature ring oscillator has wider tuning ranges and low phase errors, while operating at higher frequencies and consuming lower power. These better characteristics stem from employed feed-forward technique and positive feedback between stages with opposite phase.

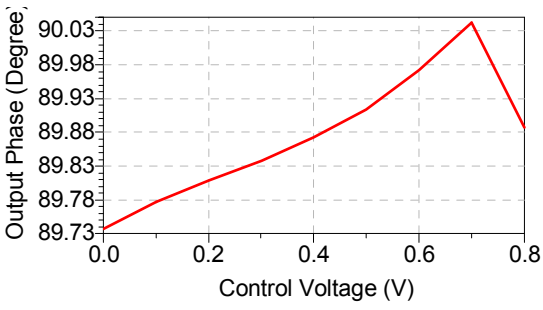


Figure 7 Output signal phase variations over 0.8 to 11.3 GHz

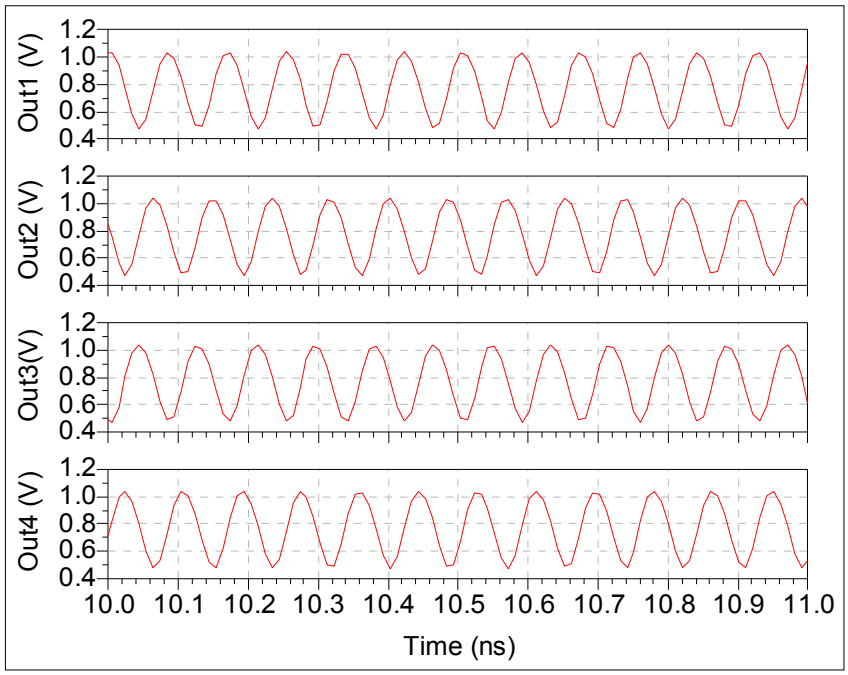


Figure 8 Time domain quadrature outputs at highest frequency

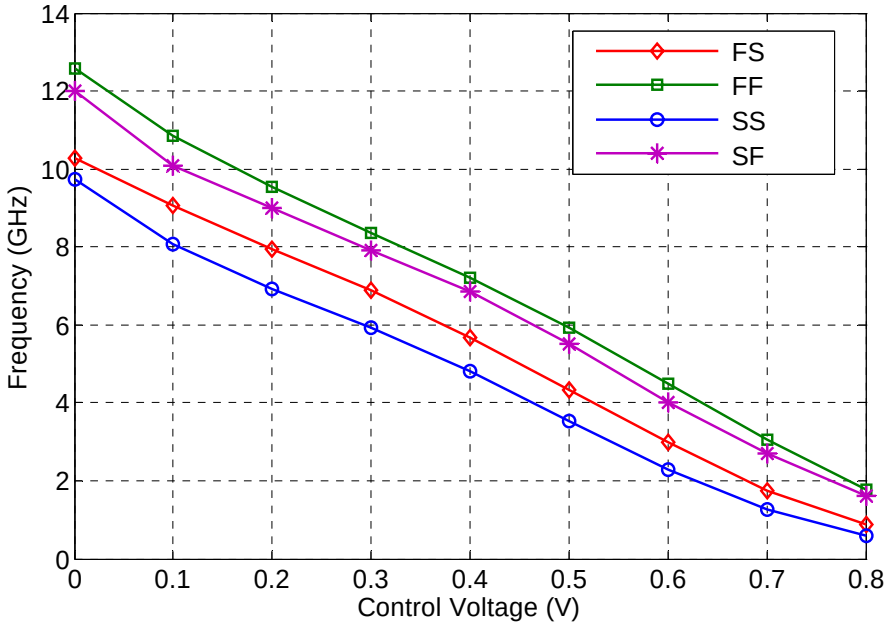


Figure 9 Oscillation frequency variation in different process corners

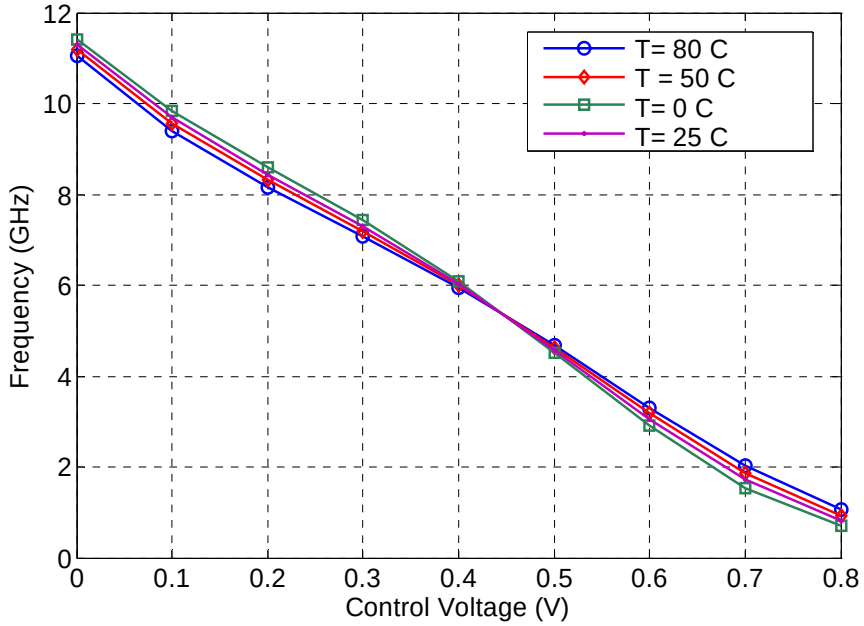


Figure 10 Frequency variations over control voltage with different temperatures

Table 1 Performance Comparison with prior state-of-art published works

| Parameter | Proposed VCO | [5] | [6] | [7] | [8] | [9] |
|---|---|---|---|---|---|---|
| Oscillator Concept | Feed forward QVCO | Feed forward QVCO | Feed forward | 2-stage QVCO | 2-stage | Feed forward |
| Center Freq.(GHz) | 6 | 1.8 | 9.2 | 10.65 | 5 | 5.5 |
| Tuning range | 175% | 180% | 18% | 16% | 130% | 14% |
| Phase noise @1MHz(-dBc/Hz) | 83 | - | 99.9 | 94.7 @ 2 MHz | 82 | 99.2 |
| Technology | CMOS 0.13µm | CMOS 0.18µm | CMOS 0.18µm | BiCMOS | CMOS 0.18µm | CMOS 0.25µm |
| Power Dissipation(mW) | 10 | - | 50 | 75 | 135 | 80 |
| FOM(dBc/Hz) | 171 | 155.3 | 174.7 | 162.5 | 155.2 | 166 |

## 5. Conclusion

In this paper, a new four-stage ring oscillator with quadrature outputs is proposed in a 0.13µm CMOS technology. This oscillator illustrates 175% tuning range @ 6 GHz. It utilizes feed-forward technique and a load with negative resistance to reduce the delay of each stage. The phase noise of the circuit is -83 dBc/Hz@1MHz offset from centre frequency, and consumes only 16mW. Monte Carlo simulation results reveal that quadrature error and phase variation are better than 0.6˚and 0.4˚ over 0.8 to 11.3GHz, respectively.

**6. References**

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