

Fault Tolerant Reversible QCA Design using TMR and Fault Detecting by a Comparator Circuit

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Abstract

Quantum-dot Cellular Automata (QCA) is an emerging and promising technology that provides significant improvements over CMOS. Recently QCA has been advocated as an applicant for implementing reversible circuits. However QCA, like other Nanotechnologies, suffers from a high fault rate. The main purpose of this paper is to develop a fault tolerant model of QCA circuits by redundancy in hardware and also identifying the faulty module by a proposed Reversible QCA comparator circuit. Triple Module Redundancy (TMR) mechanism is implemented for Reversible QCA circuits to make them more Reliable. Our proposed Comparator and Detector design uses the minimum number of clocking zones and maximizes the circuit density and focuses on a layout of the circuit which is minimal in using QCA cells. QCA Designer ver.2.0.3 is used for simulation and verifying the design.

Keywords: QCA, Reversible computing, Fault, Redundancy, TMR

1. Introduction

One of the emerging and promising nanotechnologies is Quantum-dot Cellular Automata (QCA) that has significant improvements over CMOS technology in diverse areas such as extremely low power dissipation, high operating frequency and small size [2][7]. Information in CMOS circuits is transferred by electrical current, but in QCA technology is transferred by propagating a polarization state [10].

Emerging technologies have been widely supported to replace the projected limitations of CMOS technology at the end of the roadmap [5]. Computation at nano technologies is substantially different from conventional VLSI. Extremely small feature size, high density and low power dissipation are some of the characteristics that emerging technologies must address, while implementing new Computational paradigms [8]. One of these paradigms is reversible computing. Reversible computation is obtained by establishing a one-to-one mapping between the inputs and outputs [11]. For the first time, This *bijective* property was introduced by Landauer who showed that $kT \ln 2$ joules of energy are wasted for losing one bit of information in irreversible computation, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. If computation is performed in a reversible mode, $kT \ln 2$ joules of energy would not necessarily dissipate [1]. Although currently the static and dynamic power dissipations of CMOS circuits are much higher than $kT \ln 2$ J, in the future with low power dissipation and an increased level of integration of nano-scale technologies this theoretical limit may become a major limitation [4]. Reversible

computing can be employed in nano technologies such as QCA, optical computing, quantum computing and has recently attracted substantial research attention [12].

In this paper, QCA is investigated for testable implementations of reversible logic. There is a high fault rate in QCA, like other nano technologies, thus, there is a critical need to provide devices with low error rates [14]. Defects can occur in both the manufacturing phase, which is permanent, and the operational phase, which is transient. However, at the nano-scale it is extremely hard to achieve the required manufacturing tolerances [15].

Different types of redundant scheme have been proposed and used for CMOS which are also applicable to QCA. In this paper Triple Modular Redundancy (TMR) is applied to Reversible QCA circuit as a hardware redundancy mechanism. TMR is suitable for QCA implementation since the 3-input MV is the basic logic gate in QCA and requires 5 QCA cells. TMR is only able to mask a faulty module with no detection. A Reversible QCA comparator and detector circuit is proposed to detect faulty module in the TMR system. The proposed design is optimal in using the number of cells, clocking zones, delay and speed.

2. Review of QCA

A set of four charge containers or “dots”, which are positioned at the corners of a square, is called a QCA cell [2]. The QCA cell has two mobile electrons trapped on it and they can tunnel between dots, but not cells. The electrons are forced to the corner positions by Coulombic repulsion. The two possible polarization states are considered as logic “0” and logic “1” as shown in Figure 1. Information is transferred by electrical current in conventional circuits but in QCA technology, the Coulombic interaction connects the state of one cell to the state of others. The fundamental logic gate in QCA is the majority voter (MV) [2]. The logic function of the majority voter is $MV(A, B, C) = AB + AC + BC$, which can be implemented by only five QCA cells, as shown in Figure 2b. AND and OR gates are implemented by setting one input of the majority gate permanently to “0” or “1”, which is called control input. The inverter is the other basic gate in QCA and is shown in Figure 2a. The binary wire and inverter chain are used as interconnect structures and are shown in Figs. 2c,d [4].

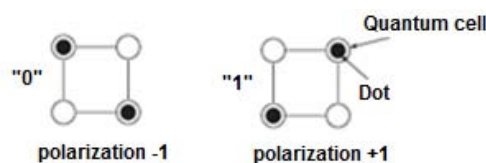


Figure 1. QCA cell and polarization states.

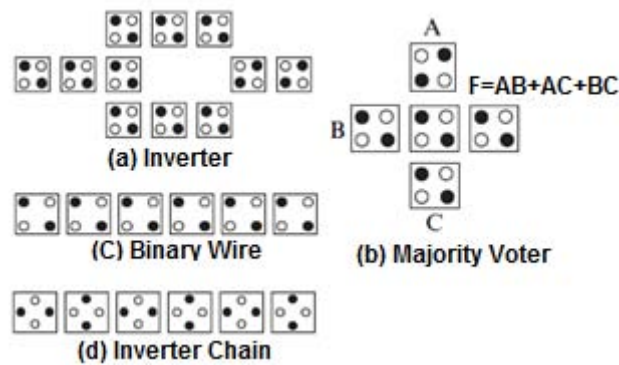


Figure 2. Basic QCA devices.

In VLSI circuits, timing is controlled through a reference signal which is called *clock* but timing in QCA is performed by clocking in four periodic phases such as Relax, Switch, Hold, Release phases [6]. During the Relax phase, there is no interdot barrier and a cell remains unpolarized. During the Switch phase, the interdot barrier is slowly raised and a definitive polarity is achieved under the influence of the neighbors of the cell. Actual computation takes place in this phase. In the Hold phase, barriers are high and the polarity is retained. During the Release phase, barriers are lowered and a cell loses its polarity. This clocking mechanism allows inherent pipelining [7][9] and obtains multi-bit information transfer for QCA implementation [4].

3. Reversible computing

Reversible computing is one of the promising technologies that do not erase information and has virtually zero heat dissipation. By definition, a system is reversible if it can operate in a backward direction. Thus, the inputs can be reproduced from the outputs. It is proved by Bennett in 1973 that no energy dissipation will occur in a system until it is able to return to its initial state from its final state and what happened in between is not important. The logic that supports the process of computing in the backward direction in the system is called reversible logic. Reversible logic is discovered by Toffoli and Fredkin in the late 70s and early 80s [17]. For any gate to be reversible, its logic function has to be *bijective*. It means that there is a one-to-one mapping between inputs and outputs and the outputs and inputs can be uniquely produced from each other. For any Reversible gate, there is a *dual*. If a reversible gate cascades with its dual, the logical operations can run backwards [21]. If there is m inputs and n outputs in the logical function, Therefore, $m = n$ is a necessary condition for a gate to be reversible [13]. Several reversible logic gates have since been proposed, including the Feynman gate, Toffoli gate, Fredkin gate Peres gate and the Margolus gate.

4. Fault Tolerance in QCA Using TMR

There is a high fault rate in the manufacturing of molecular QCA circuits, like other nano-scale technologies. To obtain a reliable computing system in QCA, Different types of redundant scheme are applicable to QCA. Faults can occur in both manufacturing and

operational phase. A potential fault tolerant technique in QCA must be able to tolerate both permanent manufacturing and operational fault rates.

TMR is used as a fault tolerant technique to make Reversible QCA circuits more reliable. TMR is suitable for QCA implementation because of Majority gate, which operates as a voting element and uses only five QCA cells.

4.1 Triple Modular Redundancy

In computing, Triple Modular Redundancy, sometimes called Triple-Mode Redundancy (TMR) is a fault-tolerant form of N-modular redundancy, in which three systems perform a process and that result is processed by a voting system to produce a single output. If any one of the three modules fails, the other two modules can correct and mask the fault.

TMR is a widely used fault tolerant technique. It can be implemented in QCA as illustrated in Figure 3. TMRs can be cascaded to further improve the system's reliability. The TMR scheme is advantageous for QCA because the 3-input MV gate is the basic QCA devices. With fault free MV gates, every stage in the cascaded TMR system improve the signal reliability to equation (1):

$$R_{out} = (R_{in})^3 + 3(R_{in})^2 (1 - R_{in}) \tag{1}$$

Where R_{in} and R_{out} are the reliability of the input and output signals, respectively. If $R_{in} > 50\%$, then the reliability of R_{out} is higher than the reliability of R_{in} in every stage of the TMR system. If the voter fails then the complete system will fail. However, in a good TMR system the voter is much more reliable than the other TMR components. The reliability of a TMR system with a non-perfect MV is shown in equation (2):

$$R_{sys} = R_{MV} * [(R_m)^3 + 3(R_m)^2 (1 - R_m)] \tag{2}$$

Where R_{sys} is the system reliability and R_m is the reliability of a module and R_{MV} is the reliability of the non-perfect MV. To improve the system reliability using TMR, it is required that $R_{MV} > \frac{8}{9} \approx 0.8889$.

With $R_{MV} > 0.8889$, modules with $R_{MV} \in \left(\frac{3 R_{MV} - \sqrt{9R_{MV}^2 - 8R_{MV}}}{4R_{MV}}, \frac{3 R_{MV} + \sqrt{9R_{MV}^2 - 8R_{MV}}}{4R_{MV}} \right)$ can have improved reliability using TMR [15].

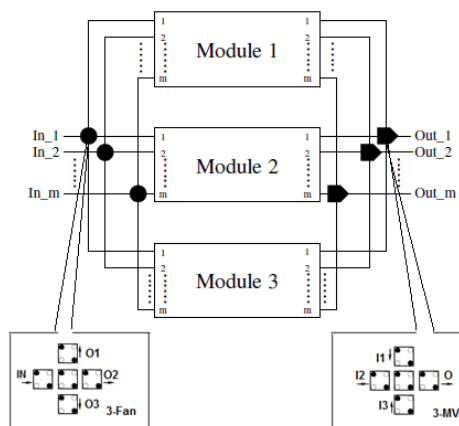


Figure 3. TMR system in QCA implementation

Modules at the TMR model can be assumed any Reversible QCA circuits such as Reversible Full adders implemented by QCA cells. Consider TMR model is only a fault tolerant mechanism that makes the system more reliable by redundancy in hardware. If there is a single faulty module, the associated incorrect output will be masked by 3-input MV gate because of other two correct inputs. TMR is only able to mask a faulty module and no detection will occur. To detect which one of the modules is faulty, a comparator and detector circuit is proposed which is reversible and implemented by QCA cells.

4.2 The Proposed Comparator Circuit Design

As previously mentioned, TMR is only able to mask a single faulty module. To detect the faulty module, a comparator circuit consists of three XOR gates is proposed. The comparator receives three output signals which are obtained by Reversible QCA modules in per stage of the TMR system and produces 3-output signals as Error Signal12, Error Signal13 and Error Signal23, as shown in Figure 4. Error signal function is introduced as follows:

$$ER_{ij} = \begin{cases} 0 & M_i = M_j \\ 1 & M_i \neq M_j \end{cases}$$

If the output of FA_i is equal to the output of FA_j, then ER_{ij} will be "0", otherwise will be "1". Figure 4. shows a stage of the TMR system that the comparator circuit is embedded for error detection. ER_{ij} represents XOR between output signals of *i*th and *j*th module. Three XOR gates are needed to compare and identify the faulty module in the TMR system. If ER_{ij} signal is "0", none of the M_i and M_j would be a faulty module. Therefore, if all of the error signals are "0", indicates no faults occur in the circuit. If a fault occurs in one of the modules, then two error signals are certainly "1" and the faulty module is one of the modules which is common between two indexes of error signals. For example if a fault occurs in M₂ in the TMR system, therefore ER₁₃ will be "0", and both of the ER₁₂ and ER₂₃ signals will be "1". Since index 2 is common, the faulty module is M₂.

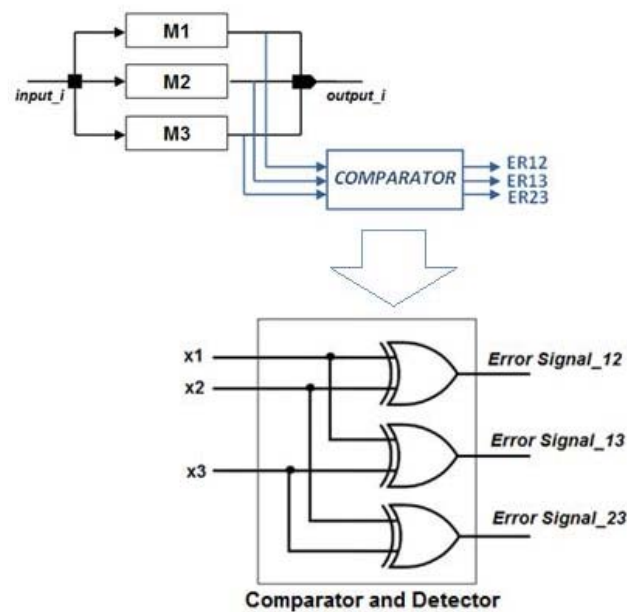


Figure 4. Schematic diagram of the embedded comparator and detector circuit

For our proposed comparator circuit to be reversible, the logic function has to be bijective. Thus a logic function is reversible if and only if there is a one-to-one correspondence between its inputs and outputs [17]. The fan-out of any output of a reversible logic gate is limited to one. That is, each output of a reversible logic gate can drive only one input of another gate. This limitation and the variety of reversible gates, makes the synthesis of reversible circuits more complicated than that of the irreversible ones [19].

[20] Introduces a broad concept of Don't Cares (DCs) in reversible logic circuits and quantum circuits. Don't Cares are classified into three categories: inputs, outputs, and conditions. When defining logical functions, there are inputs whose corresponding outputs are not determined. That is, the truth table of the function is not completely defined. Conventionally, these patterns are called "don't care conditions". In reversible or quantum logic circuits, there are also some inputs or outputs whose values are not important. These extra inputs or outputs are usually added to the circuit to make it reversible. These added inputs and outputs are called "constant inputs" and "garbage outputs", respectively [18].

Constant inputs are some inputs of a reversible or quantum circuit with arbitrary constant values. Constant inputs have two important roles in reversible circuits. They are necessary in reversible realization of an irreversible function. Since the values of constant inputs are considered "don't care", they can be used to synthesize a reversible function, efficiently [20]. In some reversible circuits, there are some outputs whose values are not important. Increasing the number of these garbage outputs increases the information loss of a reversible circuit [18].

It is proved that there is an optimum value for number of constant inputs to obtain a circuit with minimum quantum cost [19]. To make the logical function of the comparator circuit reversible, one constant input and one garbage output are added. It is defined $R=1$ and Gar output as shown in Table. 1. By Plotting the Gar expression on a Karnaugh map, it is indicated as "R3 AND X3". By adding the minimum number of

input constants and garbage outputs, the proposed circuit design is synthesized efficiently.

Table. 1. The Reversible Function of the Comparator and Detector Circuit

Constant Input	The main Inputs and Outputs			Garbage Output			
R	X1	X2	X3	ER12	ER13	ER23	Gar
0	0	0	0	X	X	X	X
0	0	0	1	X	X	X	X
0	0	1	0	X			X
0	0	1	1	X			X
0	1	0	0	X	...		X
0	1	0	1	X			X
0	1	1	0	X	X	X	X
0	1	1	1	X	X	X	X
1	0	0	0	0	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	1	0	0
1	1	0	1	1	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	0	0	0	1

Don't Care Conditions

The Irreversible Function of the proposed Comparator Circuit

QCA implementation of the proposed comparator and error detector circuit is shown in Figure 5. The proposed comparator totally applies 9 Majority gates and one AND gate. To obtain the minimum delay in the proposed circuit, the gates are implemented in a way that the input to the output gap is minimal. Four clocking zones only are used. The number of clocking zones presents the delay between inputs and outputs. We use the minimum number of gates and clocking zones to implement the design, therefore operating speed of the synthesized circuit is the more quick. Proposed implementation of the detector design uses the minimum number of gates and maximizes the circuit density and focuses on a layout of the circuit which is minimal in using QCA cells. Input wires passed over each other to ensure no interferences occur in the circuit. The proposed comparator and fault detector circuit is able to detect any masked faulty output in the TMR system in condition that only one of the produced outputs is faulty. The proposed comparator circuit should be implemented faultless.

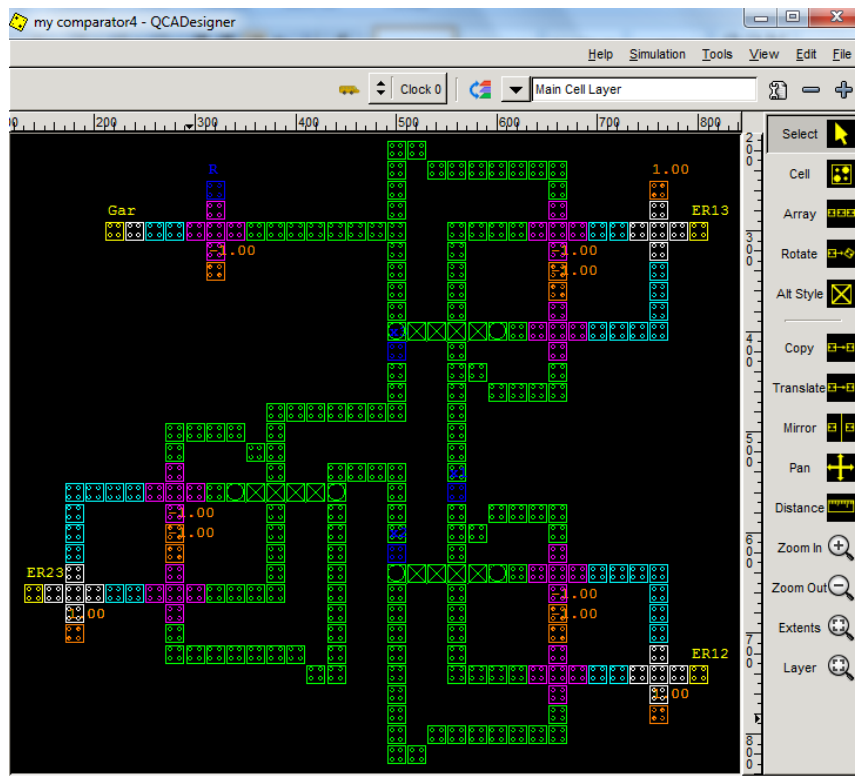


Figure 5. QCA implementation of the comparator and fault detector circuit

4.3 Simulation Results

QCA Designer ver.2.0.3 is used for simulation and verifying the design. Designer is able to rapidly design a QCA layout by QCA Designer which provides an extensive set of CAD tools [16]. All cells used in the simulation have size of $18\text{nm} \times 18\text{nm}$ and Dot Diameter size of 5nm . The four phase clocking is used in QCA design and cells in the different clocking zones are represented by different colors in circuit layout. The simulation and verification result of the proposed comparator and fault detector is shown in Figure 6.



Figure 6. The Simulation Result of the Comparator and Detector Circuit

5. Conclusion

QCA has been as an alternative for implementing Reversible computations in the recent years. On the other hand there is a quite high fault rate in nano technology. In this paper a fault tolerant model of QCA circuits is developed by redundancy in hardware. TMR model which is suitable for QCA implementation is able to mask the defective output of a single faulty module. To detect the faulty module, a Reversible comparator and fault detector circuit consists of three XOR gates is proposed. Proposed QCA implementation of the detector circuit uses the minimum number of gates and clocking zones and maximizes the circuit density and focuses on a layout of the circuit which is minimal in using QCA cells. The proposed Reversible circuit is optimal in occupied rectangular area, the number of gates, and the number of clocking zones.

6. References

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