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Optimized Reversible Programmable Logic Array (PLA)

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Abstract

Reversible logic circuits have found emerging attentions in nanotechnology, optical computing, quantum computing and low power design. A programmable logic array (PLA) is a universal circuit which is used to implement combinational logic circuits. The main part of a PLA is its AND array. In this study we propose two types of optimized reversible programmable logic array (RPLA) circuits. The first type is based on a "2-to-4" AND array, and is proposed for the first time. The second type is based on a "3-to-8" AND array. For each type, we bring some different designs. These circuits are compared with the existing counterparts in terms of number of constant inputs and garbage outputs, delay and the quantum cost and are shown that all parameters in proposed circuits are improved.

Keywords: *Optimization, Reversible logic, PLA, Genetic Algorithm*

1. Introduction

In 1961, Landauer [1] proved that irreversible processing of information result in energy dissipation regardless of its underlying technology due to the information loss. Reversible logic circuits are those circuits that do not lose any information because they allow the reproduction of inputs from observed outputs. Reversible circuits on the other hand have found promising attention in nanotechnology, quantum computing, and low power CMOS circuit design. In the past decade some reversible logic circuit synthesis methods are proposed [2,3]. We can use Genetic Algorithm (GA) to synthesize and optimize reversible logic circuits as well as quantum logic circuits [4]. GA-based methods have the ability to manage don't care conditions (DCs) [5, 6].

A reversible PLA (RPLA) is a circuit that allows implementing reversible Boolean functions in sum-of-products (SOP) form [7]. In this study some RPLA circuits are designed and optimized. The proposed RPLA circuits are of two different types. The first type is based on "2-to-4" AND array, and the second type is based on "3-to-8" AND array. For each type we bring some different designs. These circuits are compared with the existing counterparts and results are reported.

The paper is organized as follows: First, in Section 2, we explain the background including reversible logic gates, and PLA circuits. Then, in Sections 3 and 4, three designs for two-input RPLA and two designs for 3-input RPLA are presented, respectively. Evaluation of the proposed RPLA circuits is presented in Section 5.

2. Materials and methods

Before that we propose the method is used in this paper some background information is needed. These are information about reversible gates, quantum gates, and PLA circuits.

a. Reversible and Quantum Gates

A gate (circuit) is reversible if and only if there is a one-to-one mapping between its inputs and outputs [8,9]. Reversible logic gates can be implemented in various technologies such as CMOS, optical, quantum and nanotechnology. Quantum gates (circuits) act on qubits. A qubit is a unit of quantum information [9]. Since quantum gates cannot be implemented using conventional technologies such as CMOS, some other new technologies such as NMR, Ion-Trap and QCA are developed in the past decades [11].

A quantum (reversible) gate has the same number of inputs and outputs. Neither feedback nor fanout are permitted in quantum (reversible) circuits.

There exists many quantum gates such as Feynmann [9],Toffoli [8], Fredkin [12], Peres [13], Hadamard [11], V [9] and V+ [9] gates.

Some of two qubit quantum gates are shown in Figure 1. The 2×2 Feynman gate also known as controlled NOT (CNOT) is depicted in Figure 1.a. If the control input of CNOT is set to '0', the gate acts as a BUFFER gate; otherwise, it acts as a NOT gate. The Feynman gate can be used as a copying circuit to provide a copy of the signal. If the B input in Figure 1.a is set to '0' then two outputs of the Feynman gate are equal to the A input.

The V gate, also named "square root of NOT" gate ($\sqrt{NOT}$), is shown in Figure 1.b. The V+ gate is the complex conjugate transpose of V (See Figure 1.c.). The V and V+ quantum gates have some properties that are expressed in Eq. 1.

$$\begin{aligned} &V \times V = NOT \\ &V \times V^{+} = V^{+} \times V = I \\ &V^{+} \times V^{+} = NOT \end{aligned} \qquad (1)$$

These equations show that two V gates in series or two V+ gates in series are equivalent to the NOT gate; and two V and V+ in series, are equivalent to an identity or a BUFFER gate.

Toffoli and Fredkin gates [8,12] which are depicted in Figure 2 are 3×3 reversible gates. Both of them are universal, i.e. any logical reversible circuit can be implemented using these gates. The Fredkin gate acts as a controlled cross switch. If the control input of a Fredkin gate (A input) is '0', its target outputs, Y and Z, are the same as the corresponding inputs, B and C, respectively. If the control input is '1', the target outputs are swapped values of their corresponding inputs.

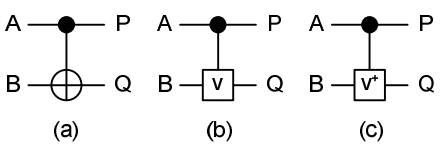

Figure 1. quantum two qubit gates (a) Feynman gate (b) Controlled V gate (c) Controlled V+ gate.

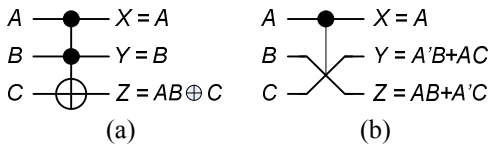

Figure 2. Most common 3×3 reversible gates (a) Toffoli gate, (b) Fredkin gate

Many other useful 3×3 gates are also proposed in the literature. Figures 3.a and 3.b show the New Gate (NG) and the Peres gates, respectively.

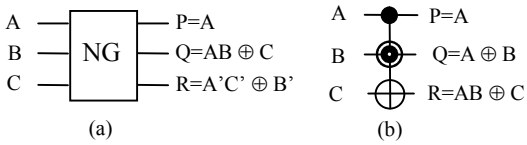

Figure 3. (a) New gate (b) Peres gate

The quantum cost (QC) of a reversible circuit is defined as the number of 1×1 or 2×2 reversible or quantum logic gates that are needed to realize the circuit [9]. For instance, the QC of Toffoli, Fredkin, and Peres gates are 5,5, and 4, respectively.

b. PLA and RPLA circuits

Logically, a PLA is a circuit that allows implementing Boolean functions in sum-of-products (SOP) form. The typical implementation consists of the AND-array followed by the programmable OR-array. The AND array realizes all the product terms (minterms) of the input variables. The OR array is used to generate various possible functions of the outputs .Figure 4 shows the structure of a traditional PLA.

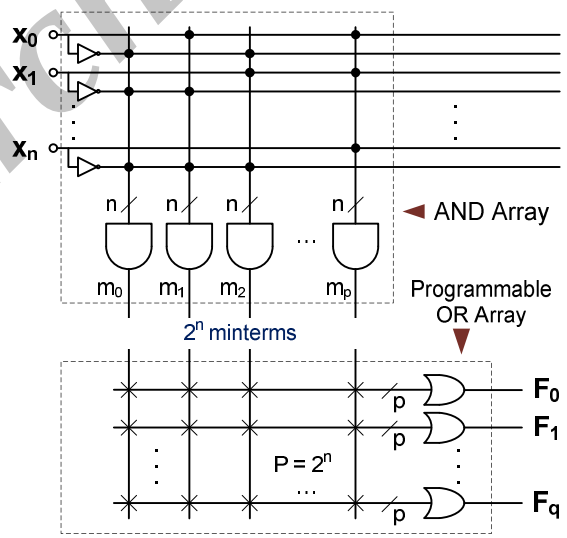

Figure 4. Structure of a PLA.

In [8] a reversible PLA (RPLA) is implemented using Fredkin gates. In the RPLA design, the bottleneck of design is the reversible AND array which have to realize all product terms of the input variables.

3. Results for Two-Input RPLA

In this section, we focus on design and optimization of the reversible AND array of an RPLA circuit. We use the genetic algorithm-based synthesis and optimization method which is proposed in [5]. This method supports "don't care values" in optimization process which results in highly optimized circuits.
The proposed designs of the AND array are of two different types. The first type is a "2 to 4" AND array, and the second one is a "3 to 8" AND array. For each type we bring some different designs.

Lemma 1: The reversible "2 to 4" AND array can be implemented using at least 4 inputs and 4 outputs, without garbage outputs and with a minimum of two constant inputs.
Proof: Traditional 2 to 4 AND array has two inputs and four outputs (Table 1). Since the output patterns are different, there is no need to use additional garbage outputs [14]. In order to make it reversible, at least two constant inputs are required. Therefore, the overall circuit can be implemented using at least 4 inputs and 4 outputs, without garbage output and with a minimum of two constant inputs ■

Table 1. Truth table of a traditional 2 to 4 AND array.

b	a	m_3	m_2	m_1	m_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

The truth table of 2 to 4 reversible AND array is shown in Table 2. It has 12 don't care conditions which are used to obtain an optimized circuit, based on the genetic algorithm-based method proposed in [5].

Table 2. Truth table of a reversible 2 to 4 AND array.

R2	R1	b	a	m_3	m_2	m_1	m_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	x	x	x	x
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	x	x	x	x

In the first attempt we use the TOFn gate library. The TOFn gate library includes TOF1 gate which is the NOT gate; TOF2 gate which is Feynman (CNOT) gate; TOF3 gate which is the Toffoli (CCNOT) gate; and etc.
Figure 5 shows the first design using this gate library. Correctness of the circuit can be verified by checking all states of inputs and outputs. It has six TOFn gates and quantum cost of 5+1+1+1+1+1=10. Referring to the Lemma 1, the number of constant inputs and

garbage outputs and overall size of the circuit are optimum. Based on the method proposed in [15], we can calculate the delay of this circuit. The delay of a Toffoli gate is 4 and delay of 2×2 and 1×1 gates is unity. Thus, the delay of the overall circuit is 9.
Using the Feynman, V, and V+ gate library, we obtain a circuit (Figure 6.a) with better specifications compared to the first design. Correctness of the circuit can be verified by applying specified values to a and b inputs and calculating the outputs, using the properties of V and V+ gates expressed in Eq.1. For example, if ba = "00", then all control inputs of V, V+, and Feynman gates are '0'. Therefore, the m0 is '1', and other outputs are '0'. If ba = "01", then the control input of the V+ and V gates are '1', the control of the Feynman gate (next to V+) is also '1'. Therefore, the V+ gate and a V gate are active which results in a Buffer gate in the m2 path. Figure 6.b shows all values of signals when inputs ba are "01". As is shown, the m1 is '1' and other outputs are '0'. The same analysis can be done for other combinations of a and b inputs.
The QC and delay of this circuit are 9 and 6, respectively. The number of constant inputs and garbage outputs and overall size of the circuit are also optimum values like the first circuit.
With different values of don't cares we obtain a different design. Figure 6.c shows this implementation which is obtained using the Feynman, V, and V+ gate library, with different values for don't cares. The number of constant inputs and garbage outputs and overall size of the circuit are optimum. The quantum cost and delay of this circuit are 9 and 6, respectively.

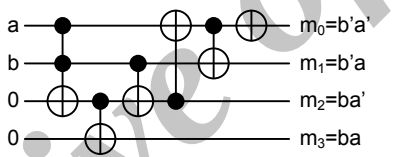

Figure 5. Design #1: The 2-input AND array circuit which is designed using Tofn gate library.

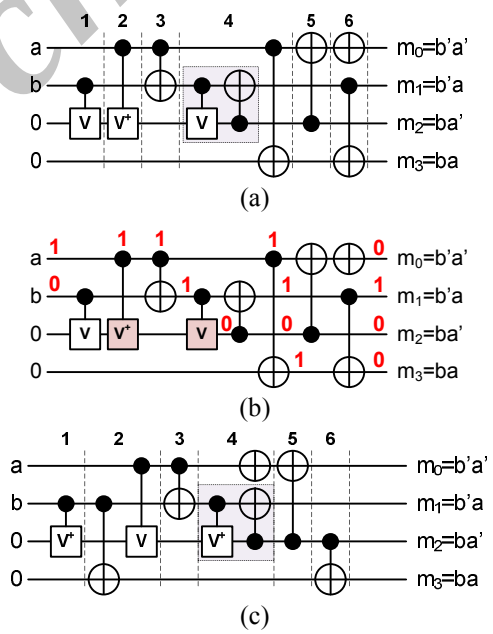

Figure 6. (a) Designp #2, (b) signal values for design #2 when ba="01", (c) Design #3.

4. Results for three Input PLA

Using the genetic algorithm-based method, we obtained two designs for 3 input AND array which are shown in Figure 7. The 3 input AND array can be used to implement the 3 input PLA circuit.

These designs use 6 Fredkin gates and one Feynman gate. The QC is 5*6+1=31 for two designs. A0, A1, and A2 are control inputs (as a binary number) and Q0 to Q7 are output "minterms" m0 to m7 , respectively.

Design #1 has 11 inputs/outputs. Design #2 is a better design because it has one less inputs/outputs. To verify the truth of these designs, we can check the outputs with different values of A2A1A0 inputs. For instance, in Figure 7.a, if A2A1A0 is "001", four Fredkin gates are in "cross" state and other gates in normal state. The '1' value in the constant input (forth line) passes through the first Fredkin gate without swapping but passes through the last Fredkin gate with a swap operation. Therefore, the m1 output is '1'. Other outputs are all '0'. The same analysis can be done for other combinations of A2A1A0 inputs.

5. Discussion

The 2-input RPLA circuit is proposed for the first time. So it has no existing counterpart in the literature and we only present the specifications of our three proposed designs. Table 3 shows these specifications. All the proposed two input AND-arrays designs use the minimum number of constant inputs and garbage outputs. The first design has QC and delay of 10 and 9, respectively, whereas, designs #1 and #2 have QC and delay of 9 and 6, respectively. Therefore, using V and V+ gates, we have 10 percent reduction in QC and 33 percent reduction in delay. Designs #2 and #3 have obtained using different values of don't cares and have the same specifications.

Table 4 shows the specifications of 3 input AND array designs. In [8, 16] the AND array is designed using a circuit with 37 constant inputs and 32 garbage outputs. The QC is 101 for this circuit. Our proposed circuits, designs #1 and #2, have 8 and 7 constant inputs, respectively, 3 and 2 garbage outputs, respectively, QC of 31, and delay of 20. Therefore we obtain 78 percent reduction in the number of constant inputs, 90 percent reduction in garbage outputs and 69 percent reduction in QC.

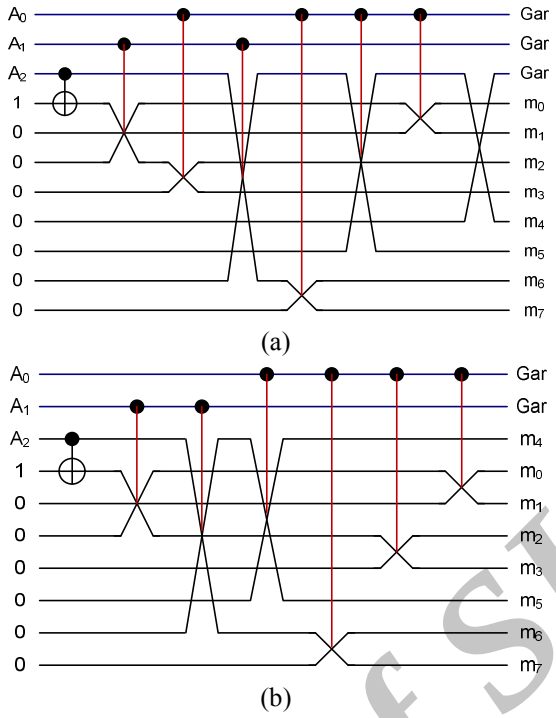

Figure 7. Proposed reversible 3-input AND arrays, (a) Design #1 and (b) Design #2.

Table 3. Specifications of 2 input AND arrays which are used in 2 input RPLAs.

Design	Gin	Gout	QC	Delay
#1	2	0	10	9
#2	2	0	9	6
#3	2	0	9	6

Table 4. Specifications of 3 input AND arrays which are used in 3 input PLAs.

	Gin	Gout	QC	Delay
[8]	37	32	101	NA
[16]	12	7	57	NA
#1	8	3	31	20
#2	7	2	31	20
% Improvement [8]	82%	94%	69%	-
% Improvement [16]	42%	71%	46%	-

6. Conclusion

In this paper we proposed some reversible circuits for 2 and 3 input PLAs. The proposed 3 input reversible PLAs (RPLAs) are compared with the existing design in terms of the number of constant inputs, number of garbage outputs, quantum cost (QC), and delay. Table 4 shows that all parameters are improved dramatically. In addition the 2-input PLAs are presented for the first time.

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