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Designing and Implementing a Fast and Robust Full-Adder in Quantum-Dot Cellular Automata (QCA) Technology

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Abstract

Moving towards nanometer scales, Quantum-dot Cellular Automata (QCA) technology emerged as a novel solution, which can be a suitable replacement for complementary metal-oxide-semiconductor (CMOS) technology. The 3-input majority function and inverter gate are fundamental gates in the QCA technology, which all logical functions are produced based on them. Like CMOS technology, making the basic computational element such as an adder with QCA technology, is considered as one of the most important issues that extensive research have been done about it. In this paper, a new QCA full-adder based on coupled majority-minority and 5-input majority gates is introduced which its novel structure, appropriate design technique selection and its arrangement make it very suitable. The experimental results showed that the proposed QCA full-adder makes only 48 cells and the first output is obtained in the 0.05clock. Therefore, the presented QCA full-adder improves the number of cells and gains a speedup rate of 33% in comparison with the best previous robust QCA full-adders. In addition, temperature analysis of the QCA full-adders shows that our design is more robust compared with other suggested QCA full-adders.

Keywords: *QCA (Quantum–dot Cellular Automata); Full-adder; Majority gate; Coupled majority-minority gate*

1. Introduction

Moore's theory that indicates doubling the number of transistors per unit area, each eighteen to twenty four months, has been persisted as a law in computer industry for more than fifty years [1]. In recent years, with smaller size of the transistors, continuing of this process has been very difficult. Thus, various technologies in order to replace with CMOS technology have been proposed. One of the six top technologies is Quantum–dot Cellular Automata (QCA) [2]. This technology is a still young technology and requires much technical work for building its circuits. Because of having Nano metric scales as well as low power consumption, it can be suggested as the best replacement for CMOS technology. The QCA technology first introduced by Lent et al in 1994[3]. Basic gates of this technology include 3-input majority function, inverter gate and wire. Since the basic computing elements, in particular full-adders are applied in different parts of computing circuits, they are considered as the most fundamental

parts of processors, which extremely affect the speed, occupied space and power consumption [4]. Thus designing full-adders with high efficiency in all technologies has always been in mind. Up to now, several QCA full-adder designs have been presented [3, 5-8], which will be discussed in section 3, precisely. In this paper, a small, fast and stable full-adder in the QCA technology based on coupled majority-minority and 5-input majority gates is introduced which has many advantages over the previous designs.

The paper structure is as follows. Background of the QCA technology has been introduced in section 2. In section 3, the related works have been presented. In section 4, the suggested QCA full-adder is described based on coupled majority-minority and 5-input majority functions. Section 5 has been allocated to performance evaluation. The results will be discussed in section 6 and finally in section 7, conclusion is produced.

2. Background

2.1 Introduction to the QCA technology

Quantum cellular automata (QCA) are a new structure that is very suitable for designing nanometer scales. The QCA cell logic is illustrated in Figure 1. As can be seen, a quantum cell can be imagined as four quantum-dots which are arranged at the corner of a square. These quantum dots are either semiconductor or very small metallic islands that are able to hold energy greater thanK_BT where K_B and $T$are Boltzmann constant and working temperature, respectively[9]. A quantum cell can exchange between the two conditions by setting the charged particles tunnel between the quantum dots mechanically. In this structure, electrons are constrained to the corner positions through Columbic repulsion phenomena. Based on how the electrons will place inside the cell, two possible polarization states will be produced, namely $P=+1$ and $P=-1$which represent the binary value of one and zero, respectively [10].

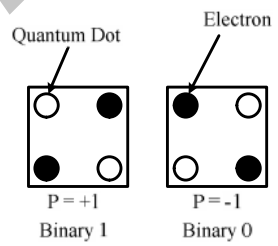
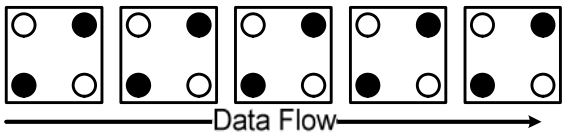


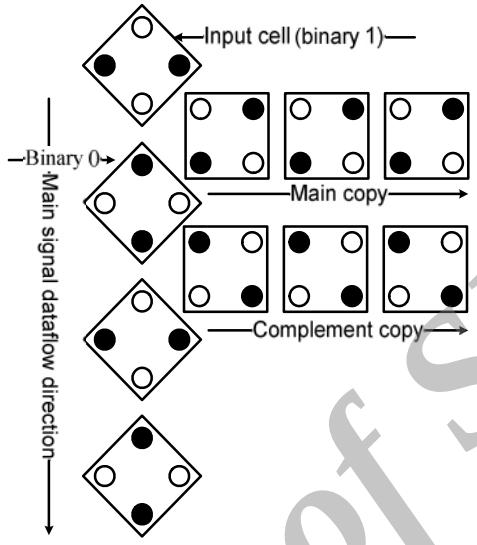
Figure. 1. A QCA cell polarization

2.2 QCA technology gates

In comparison with CMOS technology in which the binary quantities are transmitted via voltage and current on the wire, in the QCA technology, this process takes place through intercellular Columbic repulsion. Wires and gates in the QCA technology are made of the same material [10]. There are two kinds of wires: ordinary wire (90 degree) and rotated wire (45 degree), which are shown in Figure 2.



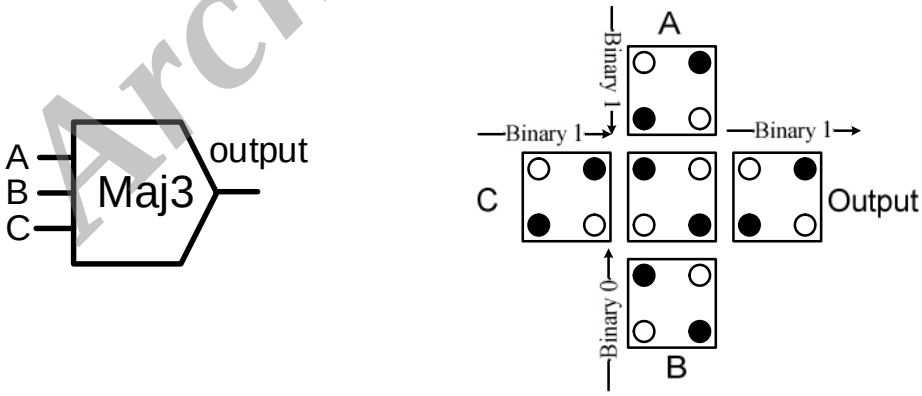
(a)



(b)

Figure.2. QCA's wire and the manner of information flow: (a) ordinal wire (b) rotated wire.

The 3-input majority function gate, where is illustrated in the Figure 3, is considered as the most important gate in the QCA technology.



(a) *(b)*

Figure.3. Three input majority function: (a) Logical design, (b) Cellular layout.

Supposing three inputs *A*, *B* and *C*, the logic function of majority gate is defined as follows:

$$M\ (A, B, C) = AB + AC + BC \quad (1)$$

In addition, Table 1 shows truth table of the 3-input majority gate.

Table 1. Truth table of 3-inpute majority function

A	B	C	Value
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Another important gate in the QCA technology is the inverter gate, which is illustrated in Figure 4.

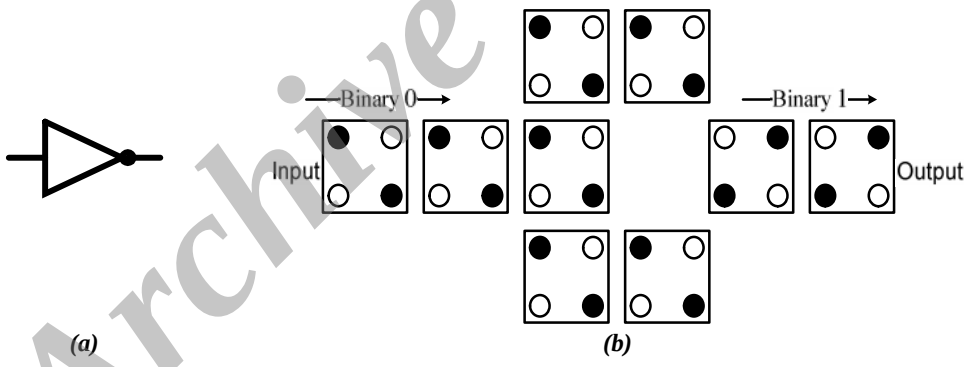


Figure. 4. Inverter gate: (a) logical design, (b) Cellular layout.

Other QCA logic circuits can be made based on wire, 3-input majority and inverter gates [11].

2.3 Clock pulse in the QCA technology

Unlike the clock pulse in CMOS circuits, which consists of an upper phase and a lower phase, the clock pulse in the QCA technology has four working phases. There is no need for any additional wiring for the clocking cells because this property naturally exists inside each cell. The clock pulse mechanism in the QCA technology gives permission for computing a sub-array. Then it blocks the sub-array as well as polarization of the output cell sets as an input for the next sub-array. Phase change is as potential change and the clock pulse phases include four states: switch, release, hold and

rest. Four zones of clock pulse and the way of emission of information in a QCA wire under the influence of clock pulse are shown in Figures 5 and 6, respectively [10].

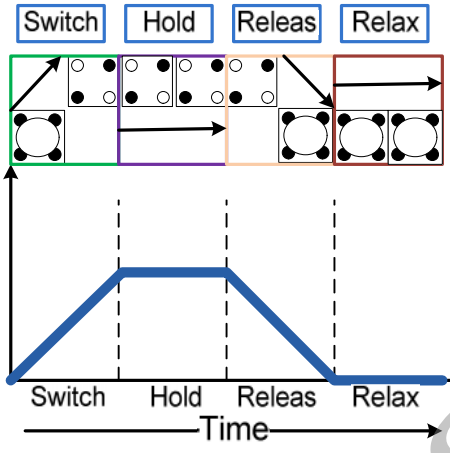


Figure. 5. Four time zones for the clock pulse in QCA and their effects on a cell

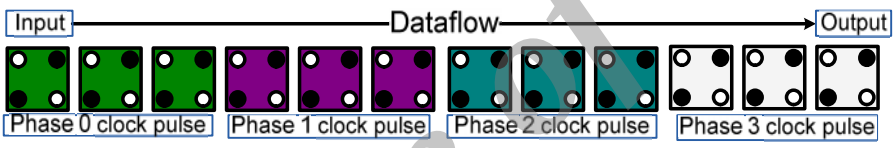


Figure. 6. How information is spread in a QCA wire

2.4 Power consumption

Power consumption in the QCA is much lower than CMOS. The QCA operation region gives per device power dissipation for QCA cells as a function of switching period. The upper bound on the QCA operation region corresponds to an abruptly switching cell, which must dissipate the full value of its kink energy about 100 mV (!) for every clock cycle. [12]

2.5 Fabrication

The QCA can be implemented by several quantum physical systems, and at least the following have been proposed.

- Metal-island quantum-dots and tunneling effect junctions
- Semiconductor quantum-dots and tunneling effect junctions
- Nano magnetic particles with single magnetic moment domain behavior
- Molecular quantum-dots

Although Cellular Automata structures have been simulated using computer software programs for a long time, the proposal of a physical realization only came in 1993 from Craig S. Lent et al, at the University of Notre Dame [13].

3. Former works on one-bit QCA full-adders

3.1 Tougaw and Lent's QCA full-adder

Tougaw and Lent's full-adder is the oldest full-adder, which includes five 3-input majority gates and three inverters [3]. This full-adder uses 192 QCA cells and its occupied area is 20 μm^2. Its logical design and cellular layout are presented in Figure. 7.

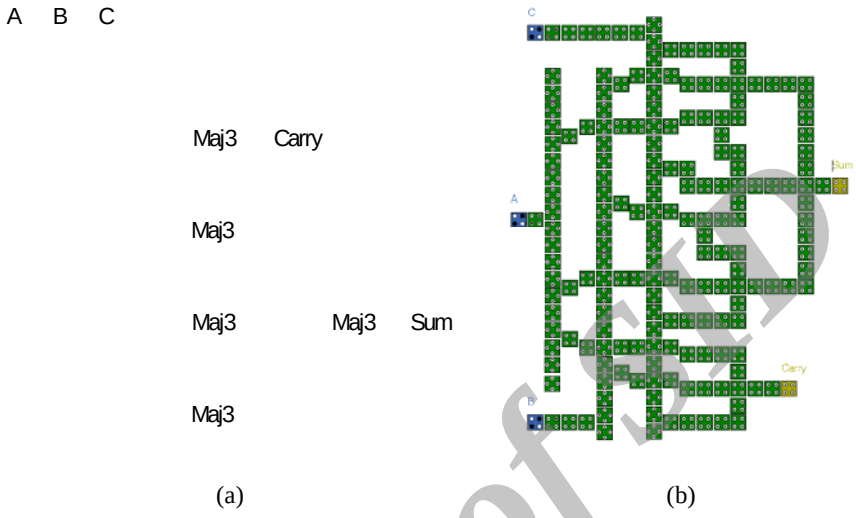


Figure. 7. The QCA full-adder presented in [3]: (a) Logical design, (b) Cellular layout

3.2 Zhang's QCA full-adder

Zhang et al introduced a new QCA full-adder, which includes three and two 3-input majority and inverter gates, respectively. The advantage of this full-adder compared with the previous QCA full-adders is the change in the structure of full-adder design based on majority gates and inverters. This design consists of 145 QCA cells and its occupied area is 0.17 μm^2 [5]. Figure 8 shows the logical design and cellular layout of the Zhang's QCA full-adder.

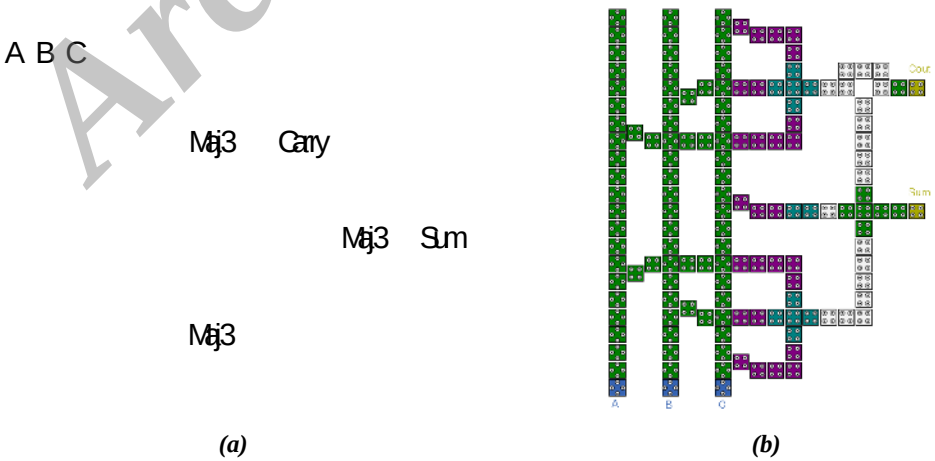


Figure. 8. The QCA full-adder presented in [5]: (a) Logical design, (b) Cellular layout

3.3 Azghadi's QCA full-adder

First time, Azghadi et al in 2007 offered a new QCA full-adder, which used 5-input majority gate to design QCA full-adder. This QCA full-adder has made up one 5-input majority gate, one 3-inpute majority gate and one inverter gate. The logical design of this QCA full-adder is shown in Figure 9. [6]

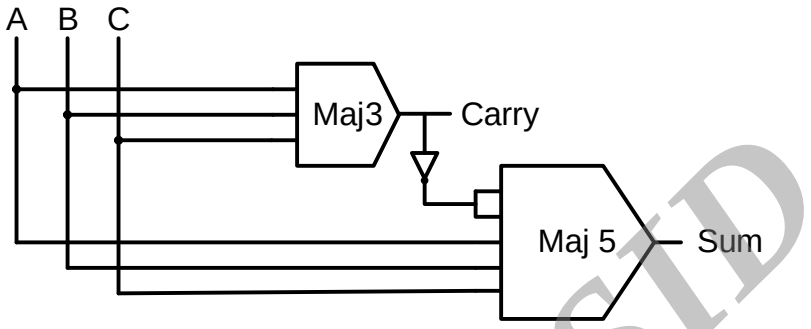
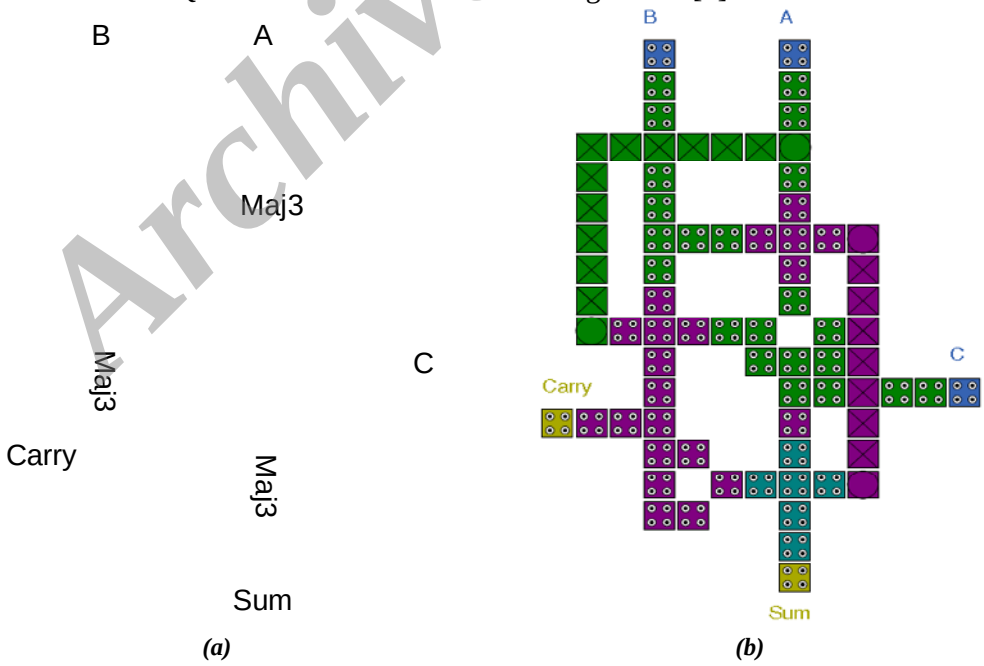


Figure. 9. The logical design of the QCA full-adder presented in [6]

3.4 Cho's QCA full-adder

Cho's QCA full-adder is known to Carry Flow Adder (CFA) [7]. This full-adder has been created with changes in the cellular layout of Zhang's full-adder. Multi layering technique has been used for producing its layout. The numbers of used cells as well as delay time have been reduced. In this design, 86 QCA cells and 0.5 μm^2 have been used. The resulted QCA full-adder is illustrated in Figure 10. [7]



(a) ***(b)***

Figure. 10. The QCA full-adder presented in [7]: (a) Logical design, (b) Cellular layout

3.5 Navi's QCA full-adder

This full-adder was presented in 2010. Though its logical design is similar to Azghadi's QCA full-adder, it uses two inverter gates in its design. First design has 61 QCA cells and its occupied area is 0.03 μm^2.The logical design of this QCA full-adder has been shown in Figure 11 (b) [14] and Second design has 73 QCA cells and its occupied area is 0.05 μm^2.The logical design of this QCA full-adder has been shown in Figure 11 (c) [8].

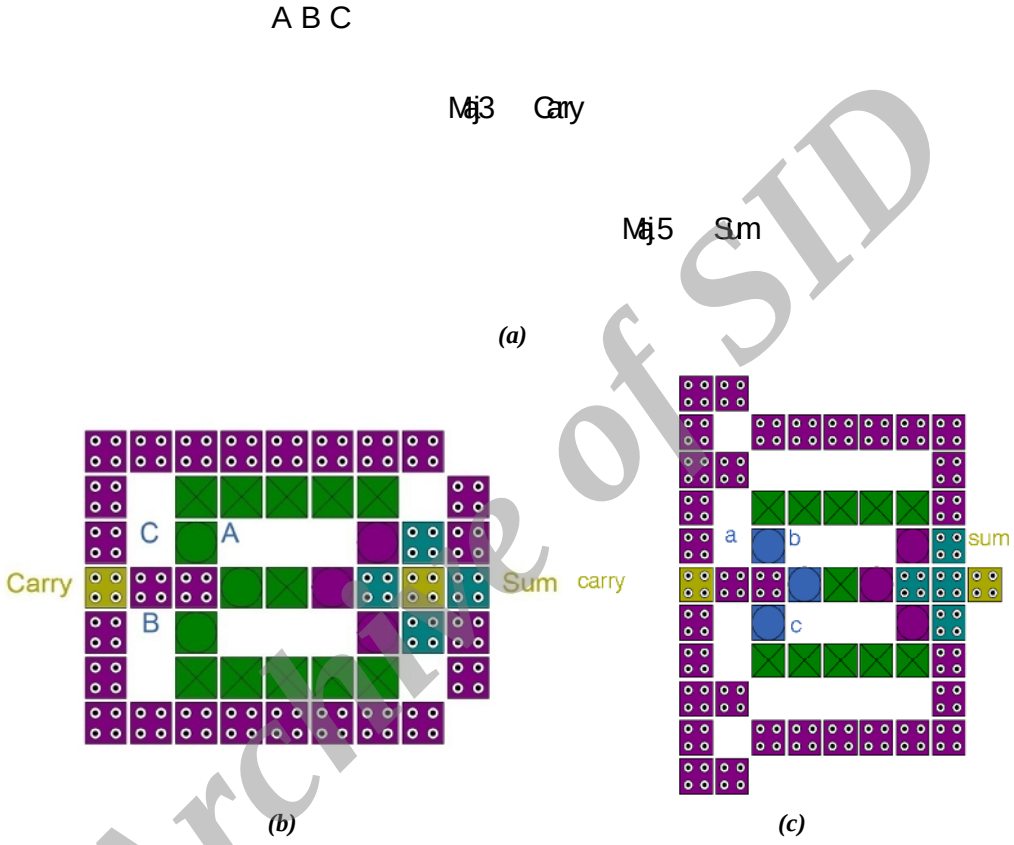
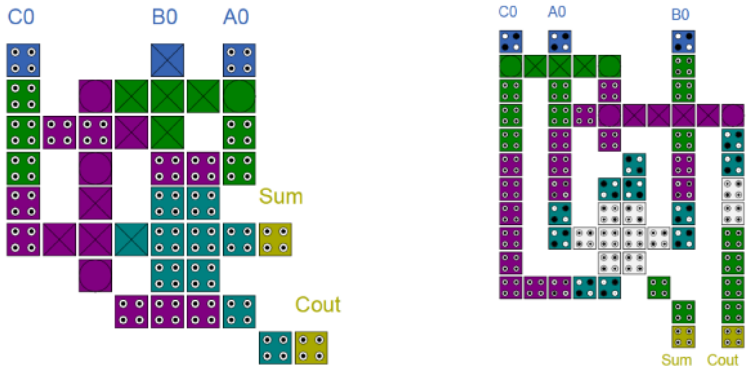


Figure. 11. The QCA full-adder presented in [8]: (a) Logical design, (b) and (c) Cellular layout

3.6 Hashemi's QCA full adder

This full-adder has been presented in 2012. Though, it's logical design is similar to Navi's QCA full-adder studied in the previous section, two cellular layouts are presented for the full adder. First design has 51 QCA cells and its occupied area is 0.03 μm^2. Moreover, robustness design has 79 cells and its occupied area is 0.05 μm^2. The cellular layout of this QCA full-adder has been shown in Figure 12 (a) and (b) [15].



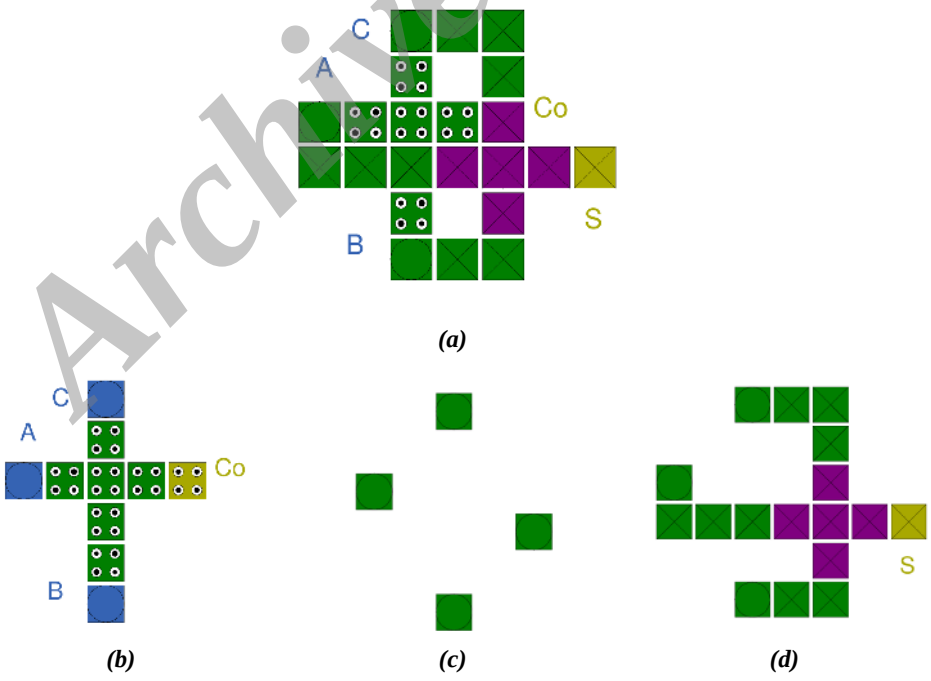
(a) *(b)*

Figure 12 The QCA full-adder presented in [15]: (a) first design, (b) Robust design

3.7 Bibhash Sen's QCA Full Adder

This full-adder was presented in 2013[16], Though it's logical design is similar to earlier full-adders [7], [8] and [15] but Bibhash Sen used new Maj5 gate that presented in [16], this full adder only has 31 cell and its occupied area is 0.02 μm^2.

Figure 13 shown Cellular design of this full-adder, because in original paper, this figure was wrong and does not produce correct outputs. We presented different layer view in figure 13. Main disadvantages of this full-adder, input cells and output cells are not in the same layer and this full-adder not robust and its fail polarization versus temperature test that we studied in section 5.3



(a) *(b)* *(c)* *(d)*

Figure 13. (a) Cellular Layout (b) Main layer (c) via layer (d) crossover layer

4. Presenting the proposed QCA full-adder

In all the previously mentioned full-adders, many times and areas in the design of adder have been used for the inverters. This issue can be noticed in a brief review of the literature, which was appeared in the previous section. Having this in mind, if these inverters are eliminated, making use of fewer cells and gaining more speed would be feasible.

For this purpose, we used one coupled majority-minority gate (CMVMIN) [17] and one 5-input majority gate [17]. Figure 14 displays our proposed QCA full-adder.

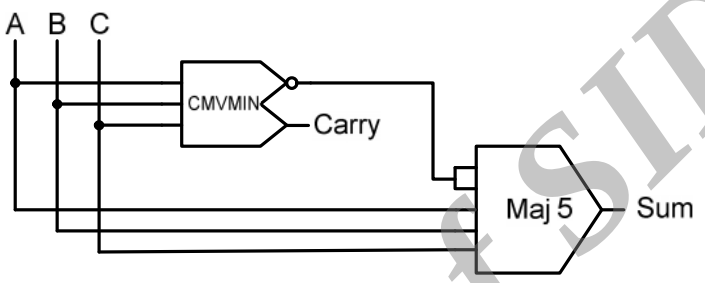
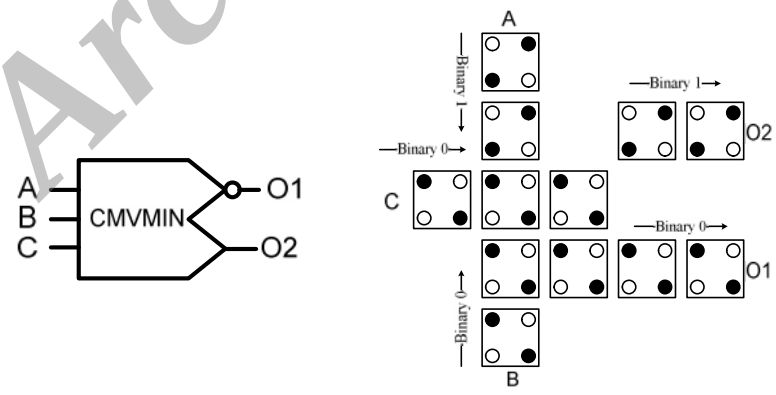


Figure. 14. Logical design of the proposed QCA full-adder

As shown in Figure 15, the CMVMIN gate has three and two inputs and outputs, respectively; where,

$$O_1 = A'B' + A'C' + B'C' \quad (2)$$

$$O_2 = AB + AC + BC \quad (3)$$



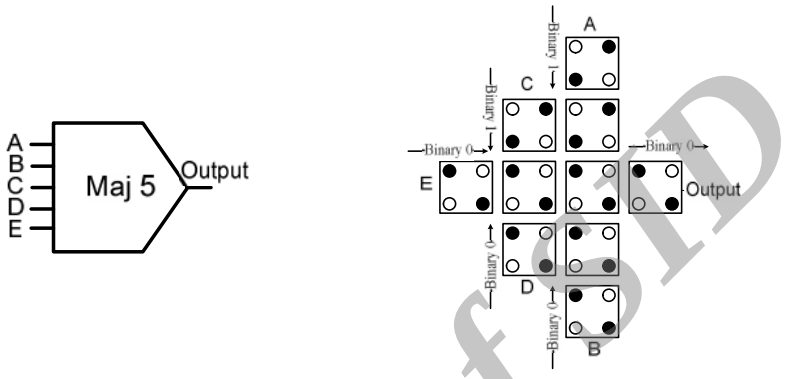
(a) ***(b)***

Figure. 15. The QCA coupled majority-minority gate [17]: (a) logical design, (b) Cellular layout.

Therefore, the carry of the suggested QCA full-adder is obtained by the output in Eq. (3).

The logical design and cellular layout of the 5-input majority gate are displayed in Figure 16. This gate operates like a 3-input majority gate. The only difference is that it has five inputs. Its logical function is also shown in Eq. (4):

$$M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (4)$$



(a) *(b)*

Figure. 16. The QCA 5-input majority gate: (a) Logical design, (b) Cellular layout.

So the sum output of the suggested QCA full-adder is obtained by the output of 5-input majority gate.

As it is obvious, the outputs of a full-adder, Sum and Carry, are computed using Eq. (5) and Eq. (6), respectively:

$$Sum = \sum m(1,2,4,7) \quad (5)$$

$$Carry = \sum m(3,5,6,7) \quad (6)$$

Although equality of equations (3) and (6) is clear, correctness of the sum output need to be explained. In the suggested QCA full-adder , besides the inputs *A*, *B* and *C*, two copies of output $O_1$from the coupled majority-minority gate, which is in fact a minority gate, are connected to the 5-input majority gate. Regarding Eq. (4), the output can be expressed as Eq. (7):

$$M(A,B,C,O_1,O_1) = ABC + ABO_1 + ABO_1 + ACO_1 + ACO_1 + AO_1O_1 + BCO_1 + BCO_1 + BO_1O_1 + CO_1O_1 \quad (7)$$

After simplifying, eliminating the repeated terms and filling $O_1$with the values from *A, B* and *C* with regard to Eq. (2), Eq. (8) is obtained:

$$\begin{aligned} M(A,B,C,O_1,O_1) = {} & ABC + ABA'B' + ABA'C' + ABB'C' + ACA'B' + ACA'C' + \\ & ACB'C' + AA'B' + AA'C' + AB'C' + BCA'B' + BCA'C' + BCB'C' + BA'B' + BA'C' + \\ & BB'C' + CA'B' + CA'C' + CB'C' \end{aligned} \quad (8)$$

As the values of the underlined expressions or terms are equal to zero, Eq. (8) can be revised to Eq. (9). In fact, this equation is the same as the sum output presented in the Eq. (5):

$$M(A,B,C,O_1,O_1) = ABC + AB'C' + A'BC' + A'B'C = \sum m(1,2,4,7) \quad (9)$$

Before discussing about the cellular the suggested QCA full-adder layout, we need to explain that, how the carry and sum outputs are achieved. As shown in Figure 17, the inputs *A*, *B* and *C* are entered into the CMVMIN gate at the first clock phase. So, the carry output is obtained at the first clock phase. For achieving the sum output, the CMVMIN output and the inputs *A*, *B* and *C* are required. Given that, the outputs of the CMVMIN gate are obtained one clock phase after the inputs, the inputs must be stored for one clock phase because the 5-input majority function inputs, must be applied simultaneously.

Considering in the QCA wiring, going to the next clock phase equals to storing the inputs for one clock phase, so that all inputs of the 5-inputs majority gate are applied to this gate in the first clock phase and the sum output achieved in this clock phase.

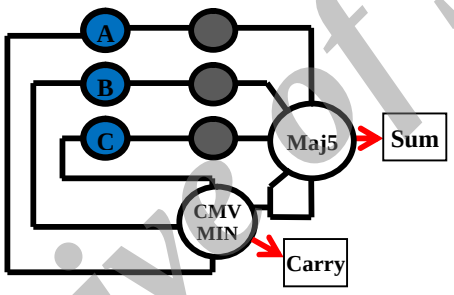


Figure. 17. The manner of generating the Sum and Carry in the suggested QCA full-adder

Cellular arrangement of the suggested QCA full-adder is shown in Figure 18. As can be observed, only two clock pulse phases have been used in this full-adder. Indeed, this is the main superiority of the proposed QCA full-adder that makes it as the fastest full-adder in the QCA technology. Moreover, this design uses only 48 QCA cells, which is the least number of cells used comparing to the former designs. It is worthy of mentioning that arrangement design of the suggested QCA full-adder has been done in three working layers and the inputs have been applied to its main layer, which is the highest layer in the arrangement[18].

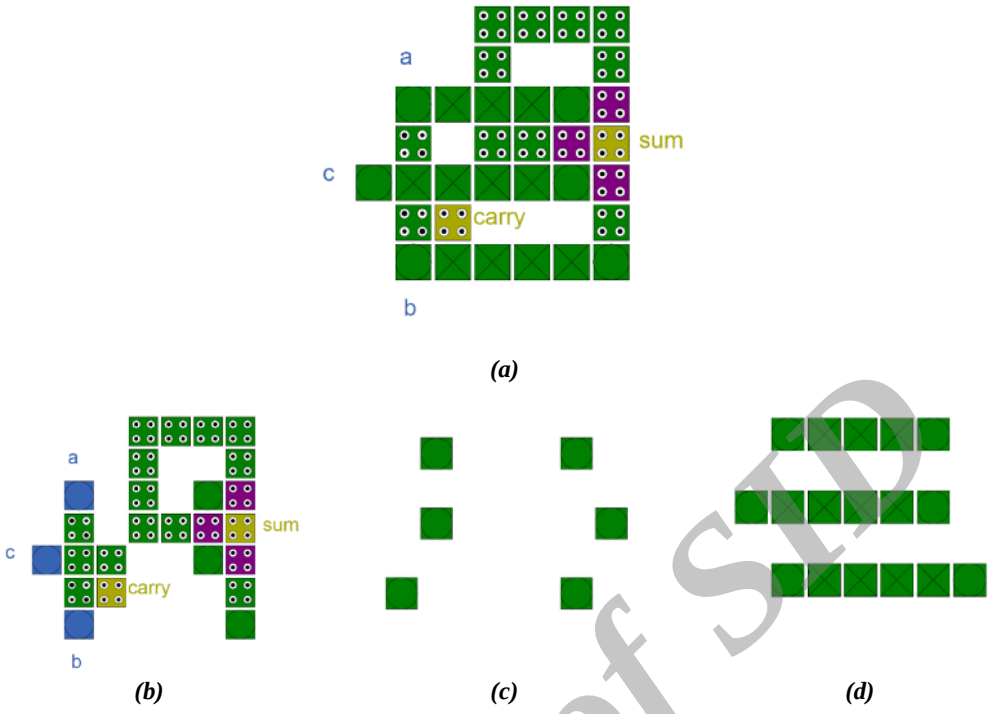


Figure 18. (a) Cellular Layout (b) Main layer (c) via layer (d) crossover layer

5. Experimental results

5.1 Simulation

To evaluate the functionality of our proposed QCA full-adder, we have simulated it by QCADesigner software 2.03, using the coherence vector engine[18, 19]. This tool makes the design, layout and simulation of QCA circuits easier and faster by supplying powerful CAD characteristics. These specifications are available in complex tools for circuit design. It should be mentioned that the coherence vector engine can model dissipative effects and carry out a time-dependent simulation of the design[19]. Similar to other simulation engines, it supposes that each cell is a simple two-state system.

The shown parameters in Table 2 have been applied for coherence vector engine. It is noteworthy that most of these parameters are default values in the QCADesigner tool.

Table 2. The used parameters for coherence vector engine

Parameter	Value
Temperature	1.000000 K
Relaxation Time	$1.000000e^{-015}$ S
Time Step	$1.000000e^{-016}$ S
Total Simulation Time	$7.000000e^{-011}$ S
Clock High	$9.800000e^{-22}$ J
Clock Low	$3.800000e^{-023}$ J
Clock Shift	$0.000000e^{+000}$
Clock Amplitude Factor	2.000000
Radius of Effect	80.000000 nm
Relative Permittivity	12.900000
Layer Separation	11.500000 nm

Simulation results of the proposed QCA full-adder are shown in Figure 19. As can be seen, the first output is obtained in the second clock phase that is equivalent to 0.5 complete clock cycles (each clock cycle consists of four clock phases).

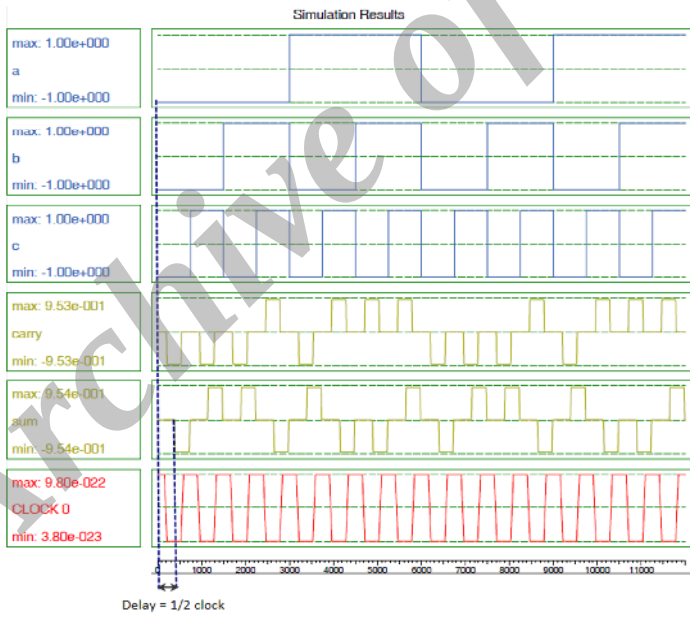


Figure. 19. Simulation results of the suggested QCA full- adder in the QCADesigner

The reason of increasing in speed or reducing in delay should be found in the following two figures (Figure 20 and Figure 21) that shows clocking map of the best previous full adder in comparison with the proposed full-adder. By replacing of marked area, the below advantages will be obtained:

1-Because of the CMVMIN gate has two outputs and also it does not use Carry output for obtaining Sum output, additional clock is not necessary and so Carry output can be obtained one clock faster.

2-As can be seen from Figure 21, obtaining minority of inputs in the zero phases causes removing one concurrency stage and therefore computational cells of 5 inputs Majority gate are located in the first phase and also the output is obtained in the same phase.

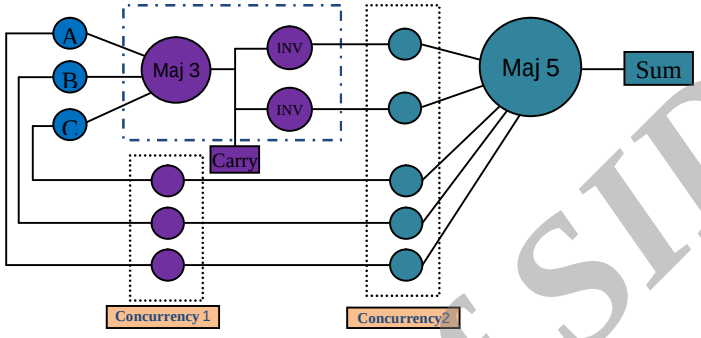


Figure 20. clocking map of Navi's adder

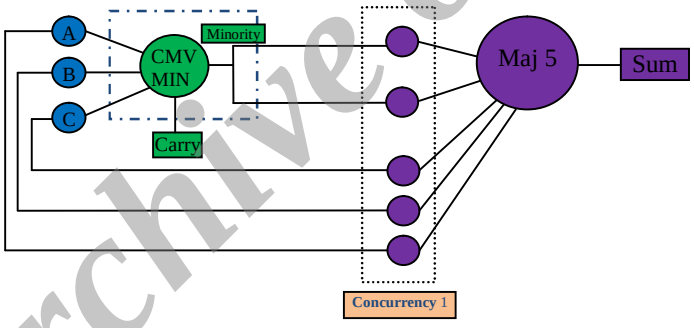


Figure 21. clocking map of proposed adder

5.2 Comparisons

Table 3 indicates a comprehensive comparison between the new suggested QCA full-adder and the previous designs from the point of view of the number of cells, area and delay parameters.

Table 3 shows the presented QCA full-adder, which uses 31 cells less than the best previous robust design. In addition, the delay of the suggested QCA full-adder is only 0.5 clock that, regarding the best previous QCA robust full-adder, shows 33% speedup. Due to our dense design, the area required in comparison with the best previous robust design is about 33% reduction.

Table 3. Comparison of the suggested QCA full-adder with other QCA full-adders presented in the literature

	QCA Full-adder	Number of cells	Delay	Area
	Tougaw and Lent's QCA full-adder[3]	192	Not applicable	0.20 μm^2
	Zhang's QCA full-adder[5]	145	5 clock phases	0.17 μm^2
	Azghadi's QCA full-adder[6]	> 200	Not applicable	> 0.9 × 2
Non Robust Design	Navi's QCA full-adder [8]	73	3 clock phases	0.05 μm^2
	Navi's QCA full-adder [14]	61	3 clock phases	0.03 μm^2
	Hashemi's QCA full-adder(first design) [9]	51	3 clock phases	0.03 μm^2
	Sen's QCA full-adder[16]	31	2 clock phases	0.017 μm^2
	The proposed QCA full-adder	48	2 clock phases	0.019 μm^2
	Cho's QCA full-adder[7]	86	3 clock phases	0.11 μm^2
Robust Design	Hashemi's QCA full-adder(Robust design) [9]	79	5 clock phases	0.03 μm^2
	The proposed QCA full-adder	48	2 clock phases	0.019 μm^2

5.3 Polarization versus temperature studies

In this section, the robustness of the suggested QCA full-adder in comparison with other designs is presented. Producing correct response with high polarization in different temperatures is called Robustness [21].

Robustness can be measured with the polarization measurement of output cells in different temperature when the circuit output is correct (temperature can be higher than the standard simulation conditions that mentioned in table 2).

As it can be observed, the polarization as a function of temperature is expressed. The polarization changes for the sum and carry outputs have been shown in Figure 22 and Figure 23 respectively. The simulation results show that all previous QCA adders except the CFA and Hashemi's adder are not able to produce correct results. Therefore, the output robustness of the proposed QCA full-adder against temperature changes has been compared with the CFA and Hashemi's adder. It should be mentioned that when the output is wrong, polarization zero has been considered.

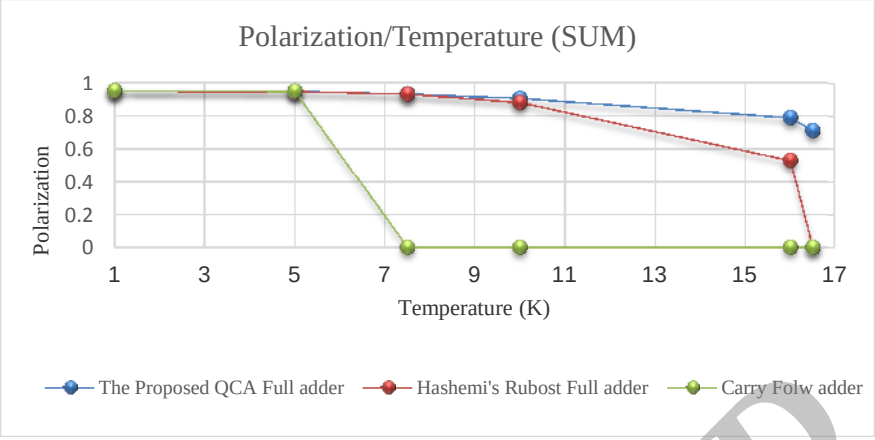


Figure 22. Polarization against the changes of temperature for the sum output

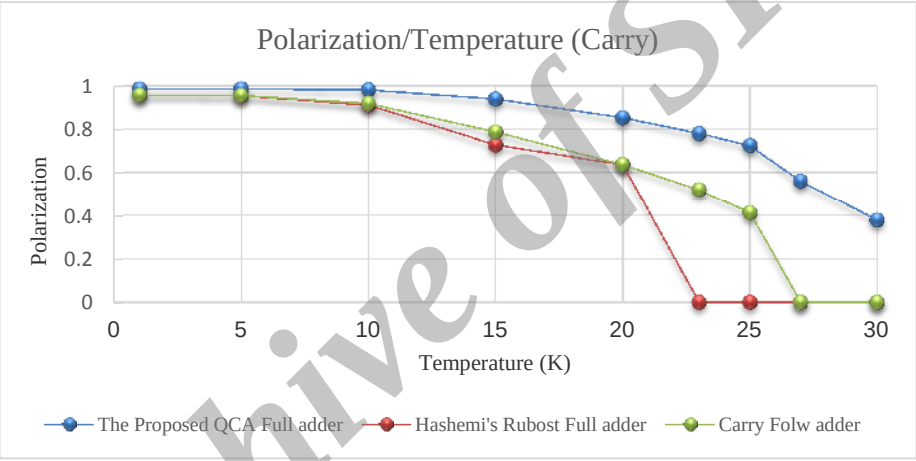


Figure 23.Polarization against the changes in temperature for the carry output

As can be observed, the performance of the suggested QCA full-adder is much better than the other ones. It should be mentioned that the outputs of the CFA Adder will' be broken down when temperature passes from 7.5 K and 27 K and Hashemi's adder will' be broken down when temperature passes from 16.5 K and 23 K, respectively. Therefore, we can deduce that the suggested QCA full-adder is so robust in comparison with others.

6. Discussion

As it has already mentioned, the proposed QCA full-adder in the present work has many advantages over the previous QCA full-adders based on the number of cells, area occupied and speedup because of its new structure as well as applying appropriate technique. Also, the arrangement of the cells in its full-adder is in the form of three-layer architecture so that, in addition to making the availability of its inputs and outputs easy by other circuits, its outputs have high emission power as well as that causes it to enjoy more robust outputs.

7. Conclusion

In This paper, a new QCA full-adder based on coupled majority-minority and 5-input majority gates is presented, which is very suitable for designing QCA circuits. The proposed QCA full-adder is able to overcome weaknesses of previous QCA full-adders due to its specific attributes. For evaluating the suggested design, we simulated it by QCADesigner software. The simulations showed very effective results on the number of cells used; areas occupied and delay, simultaneously. In addition, robustness analysis of the suggested QCA full-adder showed that it is very robust as compared with the other similar designs. This property makes the proposed design to be used in large-scale circuits as well. So in the future, it can be used in multi –bit serial and parallel adder and multiplier circuits based on full-adders.

8. References

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