Inductorless High Isolation 2.4-GHz CMOS Mixer with High Conversion Gain and Low Power

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Abstract
This paper proposes a 2.4 GHz active mixer without passive inductor for the transceiver system. Taking into account the design requirements of the mixer, a double-balanced down-conversion structure with active inductor and negative resistance is designed. The proposed mixer with 130 nm CMOS technology is designed and simulated using Cadence software at 1.5 V supply voltage. Although we had to compromise conversion gain with linearity, we were able to achieve very high conversion gain with average linearity. Based on the results of post-layout simulations, the conversion gain of 27.57 dB, IIP3 equal to -7.88 dBm, 1-dB compression point equal to -17.34 dBm and IIP2 equal to 44.22 dBm with power consumption of 2.5 mW was obtained for the proposed mixer. The chip size without input and output pads is 95.18 µm × 117.68 µm, which leads to a chip area of 0.0112mm^2.

Keywords
Mixer, frequency down converter, conversion gain, high isolation, inductorless, low power.

1. Introduction

The last few years have seen a dramatic growth in wireless communication systems. New market for high-performance receivers has made for mobile phones, laptops, and tablets with Wi-Fi and GPS capabilities and the demand in this field is increasing day by day [1]. High transmission speeds, low operating voltages, low power consumption, reduced chip area, reduced production costs and multi-standard performance have been among the most important goals of such systems [2]. In wireless communication systems, the design and development of broadband mixers has attracted considerable attention and mixers have become essential blocks in these systems [3,4].

Mixers are basically classified into active and passive groups that receive two frequency inputs and deliver one frequency output. These frequencies include local oscillator (LO), radio frequency (RF) and intermediate frequency (IF). Since the output of the mixer can be the sum or the difference between the two input frequencies, the mixers are divided into two forms of down-conversion and up-conversion. In a mixer, the RF and IF ports can be input or output, depending on the application; In the down-conversion mixer, the RF is the input port and the IF is the output port, which is the inverse of the up-conversion mixer. The LO port in both types of mixers is always the input port.

In a mixer circuit, the compromise is between conversion gain (CG), noise figure (NF), linearity (IIP3 and $P_{1\text{-dB}}$) and bandwidth (BW). To deal with the challenges and problems of compromising between the important parameters of a mixer, many efforts have been made by researchers in this field [5]. This has led to the emergence of different mixer topologies in articles, such as single-balanced mixer, double-balanced mixer, dual-gate mixer, current bleeding mixer and so on [6,7]. In the various techniques used in the articles, other parameters often get worse in return for improving a particular parameter. For example, in [8] the authors of the paper have been able to obtain an acceptable IIP3 for a wide frequency range using the dual-gate method. But this has resulted in a significant drop in conversion gain. In [9], although the high conversion gain is obtained using the current bleeding technique, but the proposed circuit in this paper may not be suitable at high frequencies. In [10] achieving a flat gain has become the cost of reducing conversion gain and losses. In [11], the bandwidth has improved but on the other hand, the conversion gain and noise figure have decreased. In [12], although the authors of the article have been able to achieve high conversion gain and acceptable linearity using the non-return to zero (NRZ) technique, the noise figure has been deteriorated and the authors have not been able to make a fair comparison with other previous articles and designs. Examples of such compromises are numerous in the articles and indicate that depending on the application, one or more parameters must be sacrificed to improve the other parameter. Therefore, it is not easy to comment on whether a mixer is good or bad [8]. Because there are so many compromises between these design criteria. In most articles, figure of merit (FOM) are defined to evaluate the performance of a mixer.

Because conversion gain is one of the most important parameters for down-conversion mixers [12], and for this

reason, in this article, we mainly focus on improving the mixer conversion gain while maintaining acceptable linearity. Therefore, we propose a double-balanced down-conversion active mixer without inductor, which increases the conversion gain by compensating with negative resistance, and also reduces the chip area due to the use of active inductor. IIP2 is improved in this paper without additional power consumption. This mixer maintains linearity (IIP3) of -7.88 dB by providing a good conversion gain of 27.57 dB.

This paper is organized as follows. Section 2 describes the proposed mixer circuit design analysis. Section 3 reports the simulation results and analysis of obtained results. Conclusions are summarized in Section 4.

2. Design of Proposed Mixer

Increasing conversion gain as well as bandwidth has always been a challenging issue in mixer design, and electronic designers have been looking for solutions to this issue. In this article, we are looking for a solution to this issue. Fig. 1 shows a schematic of the proposed down-conversion mixer. In order to perform more processing at low frequency, the higher input RF frequency is converted to the lower intermediate frequency (IF) in the down-conversion mixer. The proposed mixer is based on the basic structure of Gilbert cell, which has undergone fundamental changes in its structure to show high performance. Gilbert cell mixer due to its symmetrical topology leads to good balance in the circuit and suppression of unwanted signal components and is mostly used as a down-conversion mixer [12].

Several techniques have been considered in the proposed design, which will be described in the following. In [13] it is mentioned that by using an inductor in the mixer structure, the bandwidth of the mixer can be compensated. As we know, the use of passive inductors occupies a large area of the chip [14], and in recent years, much effort has been made to actively implement the inductors using transistors. We also used the active inductor approach for our proposed design. The active inductor we used is known as the Lu's active inductor [15]. In Fig. 1, transistors M11 to M16 implement an active inductor. Here, by biasing transistors M15 and M16 in the triode region, a voltage-controlled resistor is created, which can be changed by adjusting the gate voltage (V_b) of these two transistors. Other transistors in the structure of this active inductor are biased in the saturation region. Negative feedback in this active inductor due to the common gate operation of transistors M11 and M12 will cause an increase in voltage of node X_1 and a decrease in voltage of node X_2 to increase in the voltage of node Y_2 and decrease in the voltage of node Y_1. The source followers formed by transistors M13 and M14 ensures that the voltages of nodes X_1 and X_2 will be reduced by almost the same amount.

Assuming the passing current I_{in} from node X_1 (also, X_2) and voltage V_{in} in both nodes X_1 and X_2, the input impedance at differential port X_1 and X_2 can expressed as:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{2[j\omega(C_{gs11}+C_{gs13})-g_{m11}+g_{ds15}]}{g_{ds15}[g_{m11}+g_{m13}+j\omega(C_{gs11}+C_{gs13})]} \quad (1)$$

If $g_{m11} + g_{m13} > g_{ds15}$, then the input impedance of active inductor can be equated to an inductor L with a resistance of R_s that is parallel to a resistor R_P. Fig. 2 shows the equivalent circuit of this active inductor.

The equivalent circuit parameters of this inductor can be deduced as follows:

$$R_p = \frac{2}{g_{ds15}} \quad (2)$$

$$R_s = \frac{2(g_{ds15}-g_{m11})}{g_{ds15}(2g_{m11}+g_{m13}-g_{ds15})} \quad (3)$$

$$L = \frac{2(C_{gs15}+C_{gs13})}{g_{ds15}(2g_{m11}+g_{m13}-g_{ds15})} \quad (4)$$

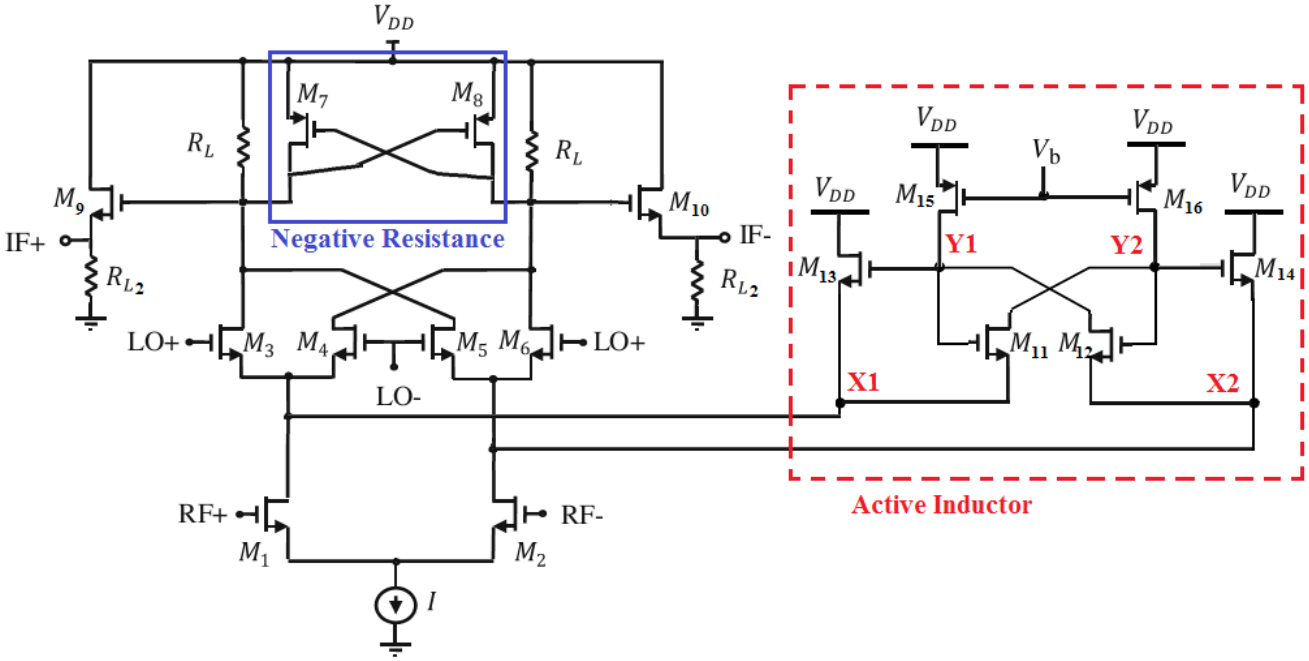


Fig.1. Schematic of the proposed down-conversion mixer

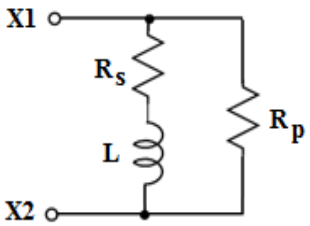


Fig.2. Equivalent circuit of the Lu's active inductor

In [16] mentioned a method to increase the conversion gain in which negative resistance compensation is used. In [16], the proposed mixer is an up-conversion mixer in which the negative resistance technique is used to increase the conversion gain of the mixer. The disadvantage of this design is the use of passive inductor, which leads to a chip area of 0.98 mm × 1.045 mm.

We have also used this negative resistance technique in our proposed down-conversion mixer. As shown in Fig. 1, the negative resistance transistors M7 and M8 provide a negative transmittance of $-g_{m7,8}$, which can attenuate the equivalent transmittance to $G_{ms,LO}$ seen from the drain terminals of M3 to M6. Therefore, with this method, the conversion interest of the mixer can be increased.

The conversion gain (CG) of the proposed mixer is given by:

$$CG = \frac{2}{\pi} g_{m1,2}(R_L || \frac{-1}{g_{m7,8}}) \quad (5)$$

Thus, the conversion gain of the proposed mixer can be increased in comparsion of conventional mixer with conversion gain of $\frac{2}{\pi} g_{m1,2} R_L$.

3. Analysis of simulation results

Simulation of the proposed double-balanced down-conversion mixer was performed using 130 nm CMOS technology for MOSFET transistors at Cadence IC Design software and the performance of the designed mixer was evaluated using various simulations. Here, we present the simulation results of the proposed mixer with active inductor and without active inductor to distinguish the performance of the proposed design with active inductor and without active inductor.

Table 1 shows all components of the simulated mixer taking into account the active inductor. For a better and fairer comparison, we simulate the proposed mixer circuit without considering the active inductor, in which case the active inductor circuit is removed and instead the real inductor with inductance equal to 1 nH and internal resistance of 5 kΩ is used.

Table 1. Components of proposed mixer

Parameter	Value
M_1-M_2	50 µm/ 0.13 µm
M_3-M_6	40 µm/ 0.13 µm
M_7-M_8	4.5 µm/ 0.13 µm
M_9-M_{10}	(100 µm/ 0.13 µm) × 2
M_{11}-M_{12}	2 µm/ 1.3 µm
M_{13}-M_{14}	(2 µm/ 0.13 µm) × 20
R_L	2 kΩ
R_{L2}	50 kΩ

In both cases, we have assumed equal power consumption for a fair comparison.

The conversion gain of a mixer determines its frequency conversion performance. The RMS voltage ratio of IF signal to RF signal is considered as the voltage conversion gain and the ratio of delivered power to load and RF input power is considered as the power conversion gain. When the mixer input impedance and the load impedance are equal to the source impedance, the voltage conversion gain and the power conversion gain will be equal. Fig. 3 shows the voltage conversion gain of the proposed mixer in terms of LO signal power, which in this figure refers to both results with active inductor and without active inductor.

According to Fig.3, the maximum value of the conversion gain, with active inductor and without active inductor, are equal to 27.57 dB and 20.84 dB, respectively. Also, the maximum conversion gain in the LO power signal are 2.132 dBm and -1dB, respectively. We will use these values in future simulations.

In practice, frequency mixing may have to be performed at a frequency that is slightly higher or lower than the predetermined frequency value. In this case, the mixer must be able to provide sufficient conversion gain, not only at a certain frequency, but also for a frequency variation [12]. For this purpose, we changed the operating frequency of the mixer from 2.4 to 2.43 GHz (variation of 30 MHz) and performed the simulation. From Fig.4, it is clear that for 10 MHz (2.4 GHz to 2.41 GHz) change in RF frequency, the corresponding changes in conversion gain considering active inductor and without inductor are only 0.25 dB and 0.5 dB, respectively. For 30 MHz (2.4 GHz to 2.43 GHz) change in RF frequency, the corresponding changes in conversion gain active inductor and without inductor are only 2 dB and 3.5 dB, respectively. Therefore, the above behavior shows the strength of the proposed circuit by considering the active inductor.

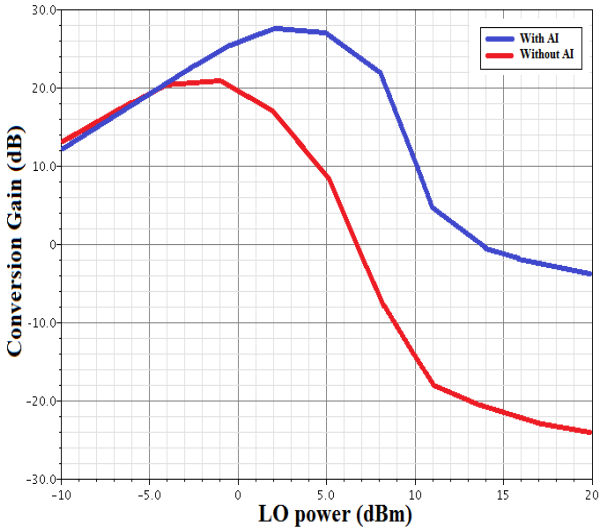


Fig.3. The voltage conversion gain of the proposed mixer in terms of LO signal power

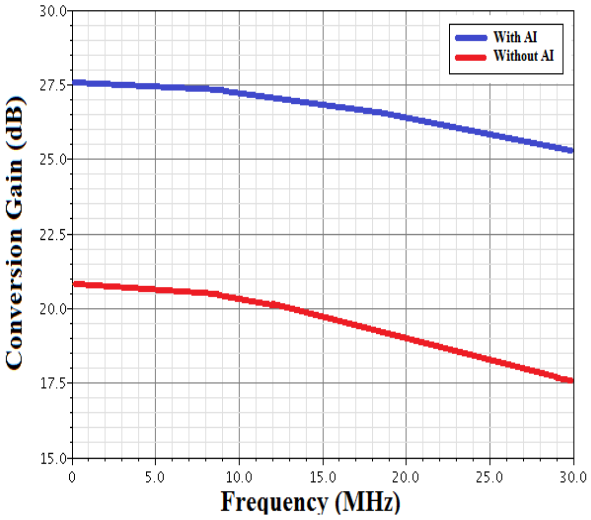
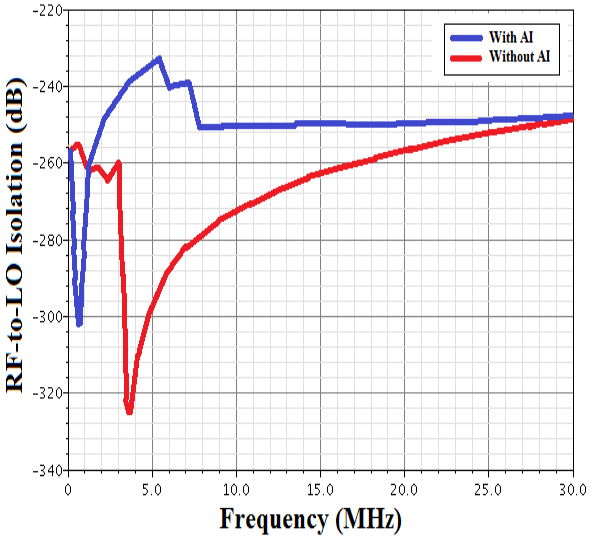


Fig.4. Voltage conversion gain of the proposed mixer in terms of RF frequency

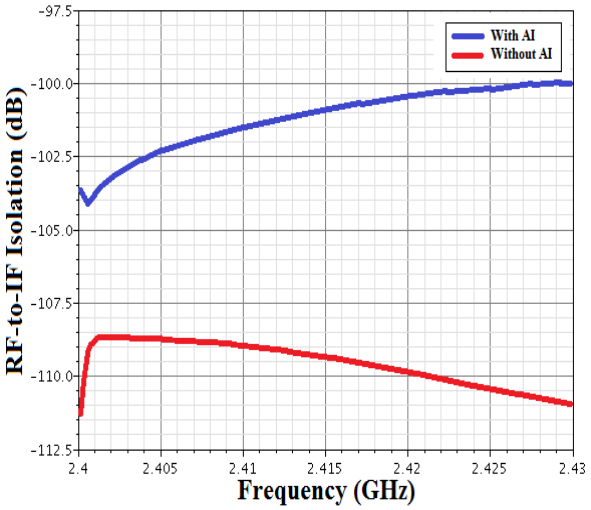
Signals may leak from one port to another through various mechanisms. LO to RF leakage causes problems in Zero-IF receivers. LO leakage may even reach the antenna via the LNA. RF to LO feed-through allows interferers in the RF signal to interact with LO. LO to IF feed-through may desensitize subsequent blocks. RF to IF feed-through causes problems in some architectures such as zero-IF. Thus, the isolation can be very important for specific mixer applications. In the following, we evaluate the isolation of RF to LO, RF to IF and LO to IF. PAC and PXF analysis in Cadence can be combined to produce a conversion function from different ports.

Fig. 5 (a) shows the isolation of RF to LO (which results in isolation below 220 dB) and Fig. 5 (b) shows the isolation of RF to IF. As shown in Fig. 5, for the case of the active inductor, we have 103 dB of RF to IF isolation. While without active inductor this value is 111 dB.

Fig. 6 (a) shows the isolation of LO to RF. According to Fig. 6, we have 95.5 dB of isolation for the case of the active inductor. While without active inductor this value is 99 dB. Fig. 6 (b) shows the isolation of LO to IF, which according to this figure we have 134 dB of isolation for the case of the active inductor. While without active inductor this value is 152 dB.

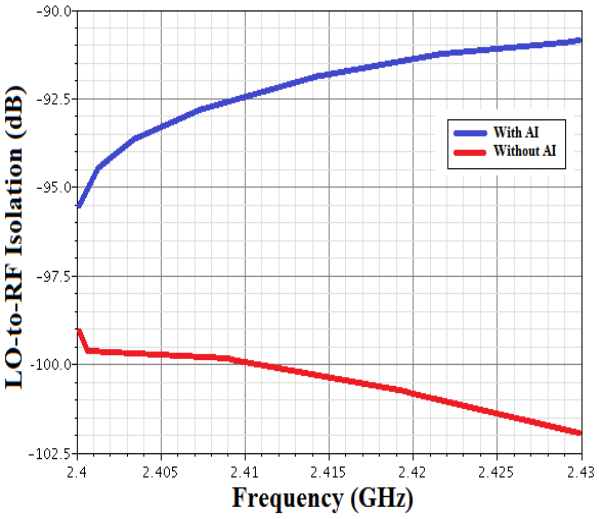


(a)

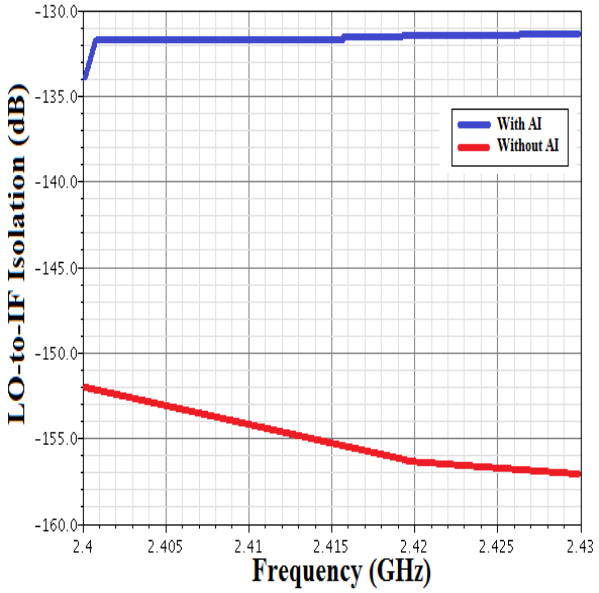


(b)

Fig.5. Proposed mixer isolation; (a) RF to LO isolation and (b) RF to IF isolation

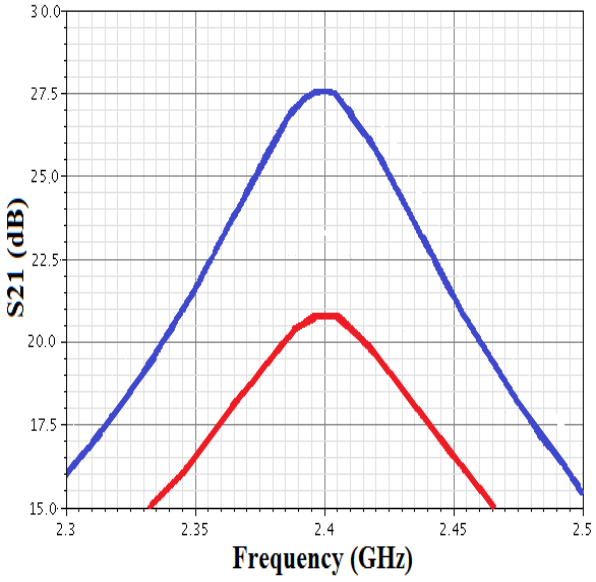


(a)

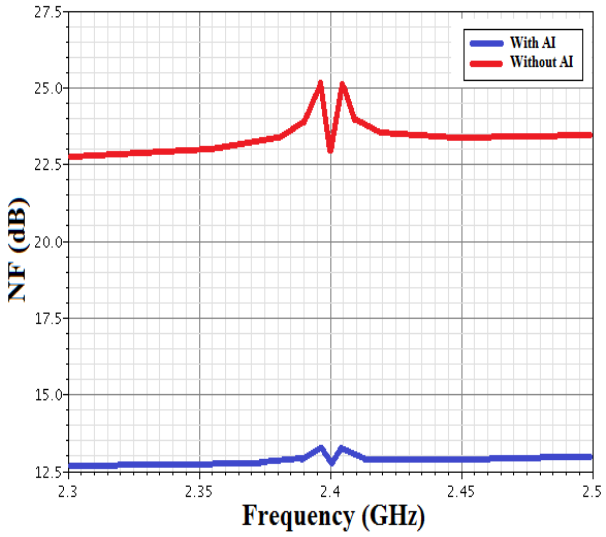


(b)

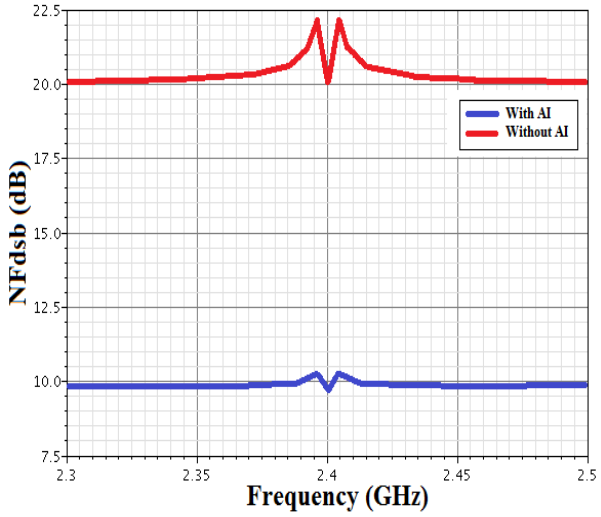
Fig.6. Isolation of the proposed mixer; (a) LO to RF isolation and (b) LO to IF isolation



(a)



(b)



(c)

Fig.7. NF and S-Parameter of the proposed mixer; (a) S_{21} and (b) NF, (c) NF_{DSB}

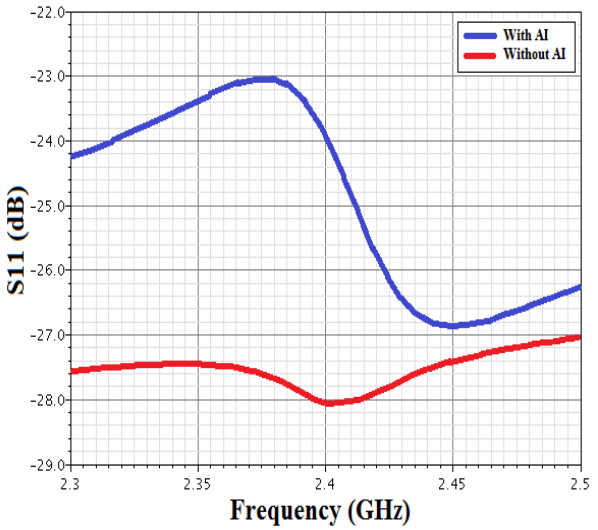
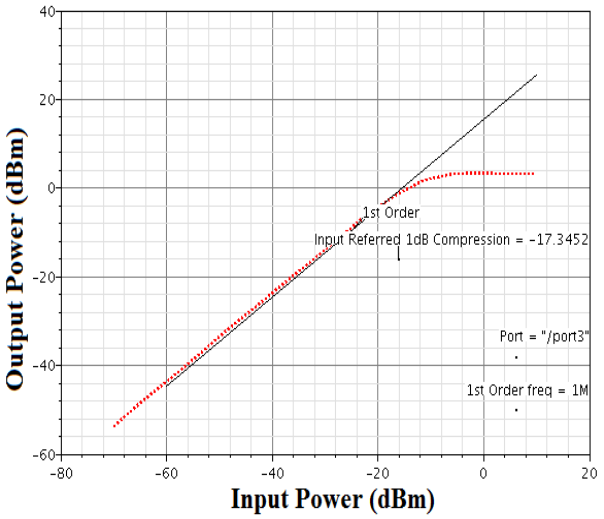


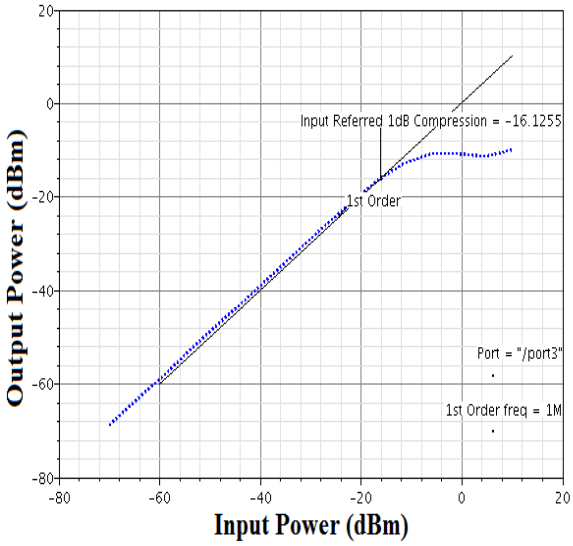
Fig.8. S_{11} diagram of the proposed mixer

Fig. 7 shows the parameters S_{21}, NF and NF_{DSB}. Accordingly, for the case of the active inductor, S_{21} is 27.57 dB, NF is 12.81 dB and NF_{DSB} is 9.8 dB. Also, for the case of the without active inductor, S_{21} is 20.84 dB, NF is 23.04 dB and NF_{DSB} is 19.99 dB. Fig. 8 shows the S_{11} diagram, which is equal to -23.88 dB for the case of the active inductor. While without active inductor this value is -28.05 dB.

In the small signal conditions, the output power increases linearly with increasing input signal power. This relationship is no longer linear when the circuits are redirected to a large signal. A 1-dB compression point ($P_{1\text{-dB}}$) is a measure of this nonlinearity. The graph for $P_{1\text{-dB}}$ is shown in Fig. 9, which shows the 1 dB compression point equal to -17.34 dBm for the case of the active inductor. While without active inductor this value is -16.12 dBm. Fig. 10 and Fig. 11 show the IIP3 and IIP2 simulation results, for the case of the active inductor, which are -7.88 dBm and 44.22 dBm, respectively. While without active inductor these values are -6.81 dBm and 46.36 dBm, respectively.

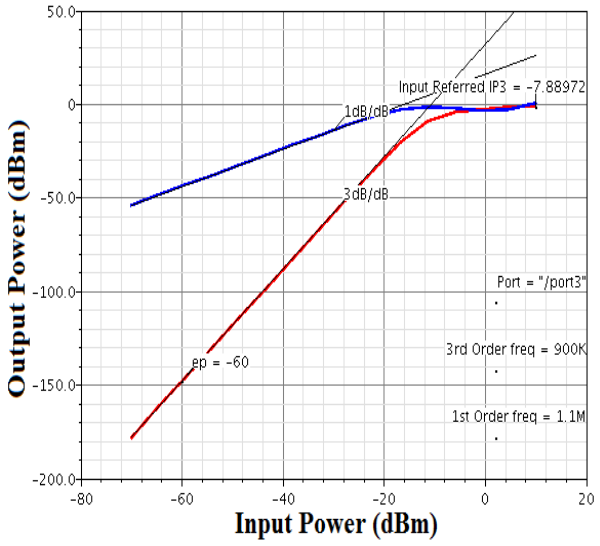


(a)

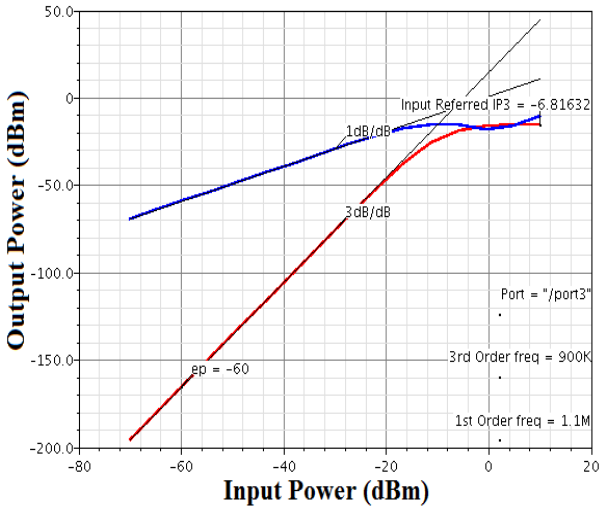


(b)

Fig.9. P1-dB of the proposed mixer: (a) with active inductor, (b) without active inductor

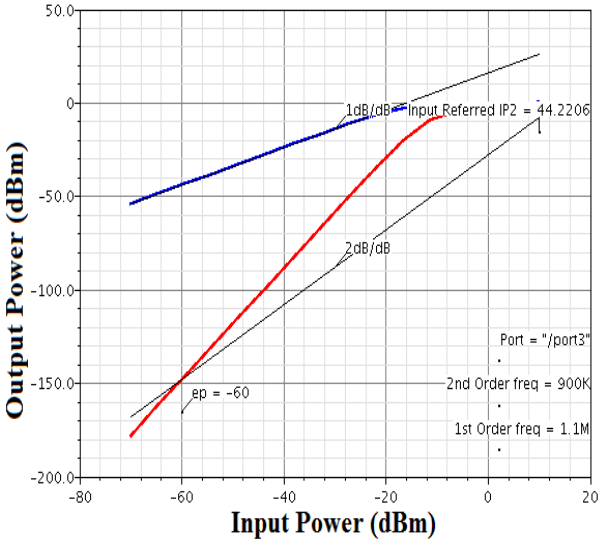


(a)

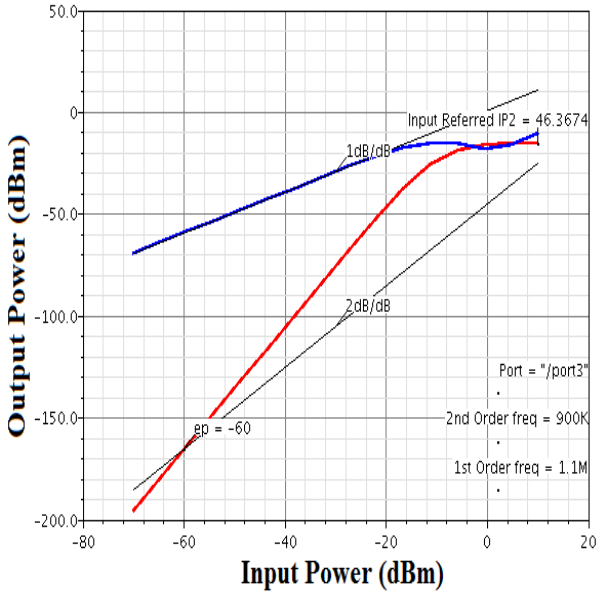


(b)

Fig.10. IIP3 diagram of the proposed mixer: (a) with active inductor, (b) without active inductor



(a)



(b)

Fig.11. IIP2 diagram of the proposed mixer: (a) with active inductor, (b) without active inductor

Fig. 12 shows the final arrangement of the proposed mixer circuit drawn in the Cadence Virtuoso environment. According to this figure, the chip size without input and output pads is 95.18 µm × 117.68 µm, which leads to a chip area of 0.0112mm^2.

Table 2 summarizes the simulation results of the proposed mixer with active inductor and without active inductor. Based on the results, it can be seen that the performance of the proposed mixer with the active inductor is comparable to the case where the active inductor is not used. The advantages of using active inductor include reducing the chip area and adjusting the mixer specifications. Changing the proposed mixer specifications for multi-standard applications is a topic that will be explored in future work.

The simulation results of the proposed mixer with active inductor and without active inductor in process corners and temperature variation, are shown in Table 3 and Table 4.

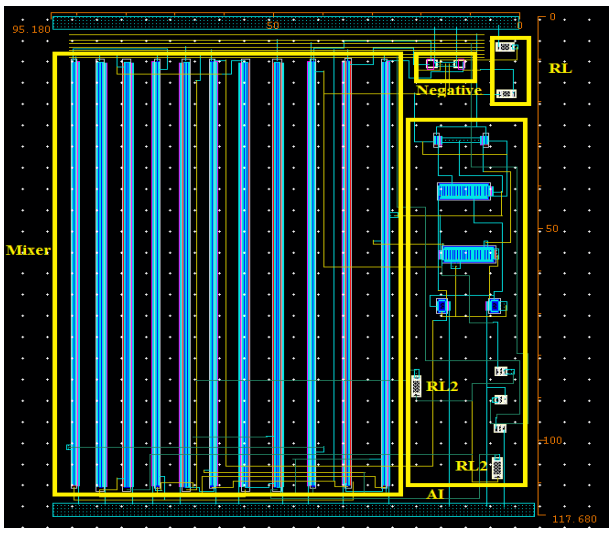


Fig.12. Layout of the proposed mixer circuit

Table 2. Summary of the proposed mixer post-layout simulation results

Parameter	Proposed with AI	Proposed without AI
Technology (nm)	130	130
Supply voltage (V)	1.5	1.5
RF frequency (GHz)	2.4	2.4
IF frequency (MHz)	100	100
Conversion gain (dB)	27.57	20.84
Power consumption (mW)	2.5	2.5
NF_{DSB} (dB)	9.8	19.99
NF (dB)	12.81	23.04
P_{1dB} (dBm)	-17.34	-16.12
IIP2 (dBm)	44.22	46.36
IIP3 (dBm)	-7.88	-6.81
S_{11} (dB)	-23.88	-28.05
LO to IF isolation (dB)	134	152
LO to RF isolation (dB)	95.5	99
RF to LO isolation (dB)	> 230	> 230
RF to IF isolation (dB)	103.5	115.5

Table 5 compares the proposed mixer with other mixer architectures previously reported in articles. From Table 5, it can be easily seen that our proposed mixer consumes much less power. Power dissipation of the proposed circuit is approximately 3.2, 6, 2.3, 7.8 and 3.1 times less than the power dissipation of the reported mixers in [13] to [21]. However, we cannot reduce power consumption by [6] and [22], but with the cost of additional power approximately 5 times, we have obtained a conversion gain of 27.57 dB that is almost 2 times the value mentioned in [6] and 1.7 times mentioned in the [22]. Although the mixer proposed in the [22] is one of the low power mixers, but the linearity characteristics of this circuit with respect to the value of IIP3 is less than the values of the items mentioned in Table 5. IIP2 and $P_{1\text{-dB}}$ simulations have also been performed, which has not been done by most authors in the articles cited in Table 5.

Table 3. Corner case simulation results of proposed mixer with active inductor

Parameter	TT 27°	FF -40°	FF 120°	SS -40°	SS 120°
CG (dB)	27.57	28.53	29.31	25.56	26.12
NF_{DSB} (dB)	9.8	6.62	12.47	9.56	14.38
NF (dB)	12.81	9.63	15.48	12.57	17.39
P_{1dB} (dBm)	-17.34	-20.74	-19.79	-16.5	-14.94
IIP2 (dBm)	44.22	38.54	37.72	44.67	49.54
IIP3 (dBm)	-7.88	-10.70	-11.13	-7.66	-5.22
S_{11} (dB)	-23.88	-24.68	-24.59	-26	-25.49
P_{dc} (mW)	2.5	2.13	2.61	1.43	1.89

Table 4. Corner case simulation results of proposed mixer without active inductor

Parameter	TT 27°	FF -40°	FF 120°	SS -40°	SS 120°
CG (dB)	20.84	21.69	22.16	19.21	19.86
NF_{DSB} (dB)	19.99	16.94	35.98	21.29	26.98
NF (dB)	23.04	19.95	38.99	24.30	29.99
P_{1dB} (dBm)	-16.12	-18.64	-14.33	-16.24	-14.01
IIP2 (dBm)	46.36	41.74	50.74	46	51.25
IIP3 (dBm)	-6.81	-9.12	-4.62	-6.99	-4.37
S_{11} (dB)	-28.05	-27.40	-26.67	-27.53	-26.97
P_{dc} (mW)	2.5	2.45	2.90	1.70	2.19

To accurately and fairly evaluate the proposed mixer with the other mixers reported in Table 5, we can use a figure of merit (FOM) by (2) depicted in [23] that the effect of conversion gain (Gain), linearity (IIP3), noise figure (NF) and power consumption (P_{DC}) is included.

$$FOM = 10\log\left(\frac{10^{(Gain+IIP3-10-2NF)/20}}{\frac{P_{DC}}{1mW}}\right) \quad (2)$$

According to the defined figure of merit, our proposed mixer has the highest FOM among the reviewed articles in Table 5. In terms of isolation, our proposed design has a very good performance compared to other designs mentioned in Table 5. Therefore, we have a very high conversion gain with the appropriate linearity profile that meets the purpose of this paper.

4. Conclusions

In this paper, the design and simulation of an active double-balanced down-conversion mixer based on Gilbert cell in 0.13 µm CMOS technology was presented. One of the main features of this mixer is the lack of inductor in the structure of the proposed mixer, which reduces the chip area. Also using the negative resistor made with two cross-coupled transistors the mixer conversion gain is well increased. The 2.4 GHz proposed mixer with a power consumption of only 2.5 mW under a 1.5 V power supply and a LO signal power of 2.132 dB achieves a conversion gain of 27.57 dB, DSB noise of 9.8 dB, IIP3 of -7.88 dBm and IIP2 of 44.22 dBm. Also, this mixer has an excellent isolation. This mixer performs better overall than the recently released CMOS active mixers. The proposed mixer with high performance is very appropriate for the modern design of the RF mixer.

Table 5. Comparison of the proposed mixer with other architectures

	[6]	[12]	[17]	[18]	[19]	[20]	[21]	[22]	This work
Tech. (nm)	130	180	180	130	130	160	65	130	130
V_{dd} (V)	0.35	1.8	1.8	1.2	1.2	1.8	1.2	1	1.5
Power (mW)	0.52	1.3	8	15.1	5.82	19.6	7.8	0.5	2.5
RF freq. (GHz)	2.4	2.4	2.1	2	2.4	0.9	0.32	2.4	2.4
CG (dB)	13.77	24.61	15	8.5	13.61	17.6	6	15.7	27.57
IIP3 (dBm)	-3.5	6.17	15	14.5	-4.46	11.8	12.5	-9	-7.88
IIP2 (dBm)	NA	82	93	NA	24	NA	NA	NA	44.22
NF (dB)	18	NA	14	17.9	20	10.1	11	18.3	12.81
IF BW (MHz)	NA	NA	NA	350	NA	100	NA	60	100
P_{1dB} (dBm)	NA	-5.86	NA	NA	NA	NA	-5.5	-28.0	-17.34
Isolation (dB)	> 55	NA	NA	NA	> 60	NA	NA	> 33	> 95
Area (mm^2)	1.03	NA	NA	0.42	0.12	0.44	1.62	0.8	0.0112
FOM	14.97	-	16.96	6.81	1.9	16.67	14.32	13.06	18.05

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