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Research Paper

Impact of Sampling Frequency on Implementation Cost and Performance of FPGA-based Digital Controller of Power Converters: Case Study for Three-Phase Four-Legs Inverters

A. Hamidi*(C.A.), S. Karimi**, and A. Ahmadi***

Abstract: One of the problems in digital control of power converters is calculation time in each sampling instant which effect on cost and complexity of digital controller. In this paper, a formula is introduced for calculating the number of clock cycles in each sample then interaction between sampling frequency and implementation cost (number of functional units and word length) of FPGA-based digital controller of DC-AC converter (three-phase four-legs inverter) is verified. The digital architecture is built on finite set model predictive control, and implemented on the FPGA board based on fixed-point calculations. We consider two digital architectures for design the controller in this study. One with four functional units and another with six functional units. This study aims to develop a mathematical equation for the number of clock cycles in each time instant to select the best switching state in the control algorithm, which affects the sampling frequency and clock frequency. Based on the obtained results, the number of functional units, word-length, and the number of switches determine the maximum clock cycles. By knowing maximum clock cycles the maximum sampling frequency is determined. In structure with four functional units, the maximum sampling frequency is 71 kHz for WL=8 bits and 17.7 kHz for WL=32 bits, and in structure, with six functional units, the maximum sampling frequencies are 97.6 and 24.4 kHz for WL=8 and WL=32 bits, respectively. In architecture with more functional units, we have greater sampling frequency with more accuracy and cost. The results obtained from this paper can be a reference for digital controller design.

Keywords: Sampling Frequency, Digital Architecture, Functional Units, Word Length, Implementation Cost, Three-phase Inverter.

1 Introduction

THE sampling frequency of A/D converters is a restriction that causes a delay in the output of digital controllers.

The efficiency and performance of a digital control system are considerably dependent on the sampling frequency. In most power electronic applications, low sampling frequency effectively degrades system performance. The lower sampling frequency is limited by the Nyquist rate and the upper sampling frequency is confined by hardware resources.

Power converters have many applications, containing drives, energy conversion, power supplies, and distributed generation. In resent, the control of these converters has been considered, and new digital controllers are presented every year [1]-[3]. Digital processors are a well candidate to control these circuits [4], [5].

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A lot of studies have been reported about the effect of sampling frequency on the performance and stability of converters. In [6], the effect of sampling frequency on the performance of a three-phase PWM inverter in a variable frequency drive, for speed control of an induction motor was analyzed. In [7], the authors discussed the theory and presented experimental results to demonstrate the effect of sample time and sampling instant on the behavior of the zero of the linear approximation of the boost converter. The effect of sampling on digitally implemented hysteresis current control in a voltage source inverter using the sampled-time-domain analysis was investigated in [8]. In [9], the effect of the sampling frequency of A/D converter on controller stability and bandwidth of digital-controlled power converter are explored. There is a variety of previous research about the analysis of sampling frequency in power converters [10]-[15]; but in general, they do not consider the effect of sampling frequency on word-length and implementation cost of digital controllers.

Our research team has done some works in this regard in recent years [3, 16, 17, 18, and 19]. We found out there are important factors that affected the accuracy of output results and digital controller implementation cost. One of these factors is the sampling frequency.

In this paper, we aim to study the impact of sampling frequency on the constraints that arise for word length and implementation cost of fixed-point implemented digital controller for a three-phase inverter. For this goal we present a new formula for calculating the number of Clock Cycles (CC) in each sample time.by knowing this number we can compute the calculation time for each instant. The control scheme is Finite Set Model Predictive Control (FS-MPC). The digital architecture is completed on an FPGA chip. The FPGA is elected because of soft architecture, parallel calculations, and high-speed execution. Then for demonstrating the sampling effect we consider different word-lengths with different sampling frequencies. Here the meaning of cost is the number of functional units and area (slice) usage in the FPGA platform. Two architectures with four and six functional units are considered for the digital controller. The number of functional units, Word Length (WL), and the number of switches determine the maximum clock cycles. By knowing maximum clock cycles the maximum sampling frequency is determined.

The rest of the paper is organized as follows. In Section 2, the effect of sampling frequency on digital architecture is verified. In Section 3, inverter structure and output signals are analyzed. In Section 4, a sampling frequency analysis of digital controller design is presented. In Section 5, results are covered and the conclusion is presented in Section 6.

2 Effect of Sampling Frequency on Digital Architecture

The sampling frequency of signals considerably changes the proficiency of digital processors as depicted in Fig. 1. In this figure, the analog signal, $x(t)$ is sampled in the period T_{sample} as $x(kT_{sample})$ and the sampled signal, $x(kT_{sample})$, is held by a zero-order hold (ZOH) as $x^*(t)$. The mediocre of signal $x^*(t)$ lags the main signal $x(t)$ by $\frac{T_{sample}}{2}$. In Fig. 1(b), the analog signal, $x(t)$, is sampled in the period $\frac{T_{sample}}{2}$ which is smaller than the period T_{sample} in Fig. 1(a). As the conclusion, the mediocre of signal $x^*(t)$ lags $x(t)$ by only $\frac{T_{sample}}{2}$ [13]. A significant increment in sampling frequency of A- to- D converter is a possible answer to tackle with this subject as shown in Fig. 1 (b). Although, as displayed in Fig. 1 (b), there is a delay among main and sampled signals although the sampling frequency, $\frac{1}{T_{sample}}$ is too high.

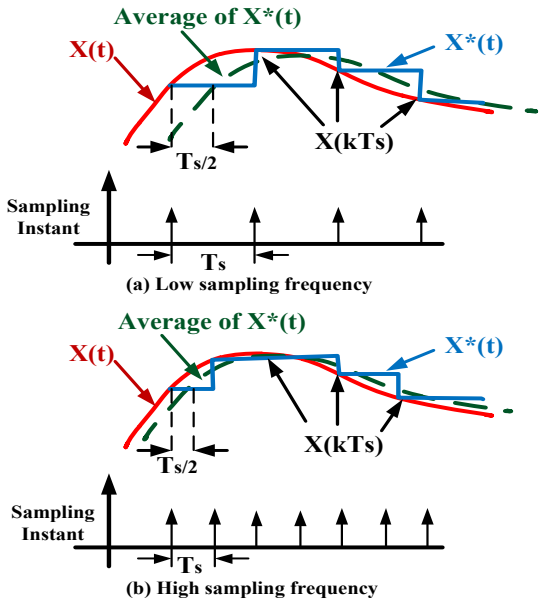

Fig. 1 Impact of sampling frequency on the digital architecture.

3 Inverter Structure under Study

A three-phase two-level four-leg inverter is displayed in Fig. 2. In this figure S_u, S_v, S_w and S_x are the switching states that are elected by the digital architecture. The control technique which is applied is FS-MPC. The most significant benefits of FS-MPC are:

- Control of complex structures.
- Removing the modulator section.
- The cost function can be determined according to the user's requirement.
- The control of linear and nonlinear schemes is feasible.

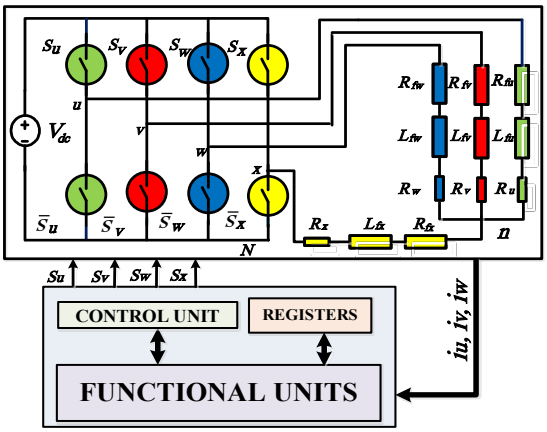

Fig. 2 Three-phase four-leg inverter and its digital controller.

FS-MPC is appropriate for circuits with discrete quiddity. Thus, since the switching power converters are studied in a discrete area, the FS-MPC is a very strong method for control these circuits. A FS-MPC structure in a three-phase inverter is represented in Fig. 2. As claimed by this scheme, load currents have been sensed and in the functional unit, according to the mathematical equations the next value for these currents will be predicted. Because the quantity of switches is 4, there are 24 switching states. In the cost minimization section by using cost function for all switching states, the state which minimizes cost function is eventually elected and applied to switches. The gate signal is depicted in Fig. 3.

The discrete state of the predicted load current is given by:

$$v_{mN} = s_m v_{dc} \ , \quad m = u, v, w, x \tag{1}$$

$$v_{mN} = (R_{fm} + R_m) i_m + L_{fm} \frac{di_m}{dt} + v_{nN} \ , m = u, v, w \tag{2}$$

$$\frac{di_m}{dt} = \frac{1}{L_{fm}} [(v_{mN} - v_{nN}) - (R_{fm} + R_m) i_m], m = u, v, w, x \tag{3}$$

According to Eqs. (1) and (3), the load neutral voltage V_{nN} can be stated as follows:

$$V_{nN} = L_{eq} v_{dc} \sum_{m=u,v,w,x} \frac{S_m}{L_{fm}} - L_{eq} \sum_{m=u,v,w,x} \frac{R_{fm} + R_m}{L_{fm}} i_m \tag{4}$$

$$L_{eq} = \left(\sum_{m=u,v,w,x} \frac{1}{L_{fm}} \right)^{-1} \tag{5}$$

$$\sum_{m=u,v,w,x} i_m = 0 \tag{6}$$

$$\frac{di_m}{dt} = \frac{i_m(k+1) - i_m(k)}{T_s} , , m = u, v, w \tag{7}$$

T_s is sampling time.

By concluding from the above equations, the discrete state of the predicted load current is:

$$i_m(k+1) = \frac{T_s}{L_{fm}} [(v_{mN} - v_{nN}) - (R_{fm} + R_m) i_m(k)] + i_m(k) \ , m = u, v, w \tag{8}$$

where R is load resistance, T_s is sampling period, R_f and L_f are filter resistance and inductance, respectively, and i_m is predicted load current.

The error for each input can be defined as:

$$e_m = i_m^*(k+1) - i_m(k+1) \tag{9}$$

Where, i_m^* is the reference load current. The cost function is computed by:

$$g = \sum_{m=u,v,w} |e_m| \tag{10}$$

The FS-MPC flowchart is shown in Fig. 4. It has five major steps that can be brief as follows.

1) Measure load currents.
2) Predict load currents.
3) Compute cost function for any prediction.
4) Elect switching state that minimizes the cost function.
5) Exert new switching state.

The load current under unbalanced load situation with a reference current 9 A is displayed in Fig 5. Other details of the circuit are represented in Table 1.

4 Sampling Frequency Analysis of Digital Control Design

As explained in prior portions, predictive control, along with all the benefits it has, needs a high-speed controller for execution that causes to much higher hardware supplies. In this control technique by calculating the intricate and long mathematical formulas, the schemes will be controlled. So, in this method, the number of hardware resources and execution cost of digital architecture are the challenges. One of the factors

which affected the hardware resources is the sampling frequency.

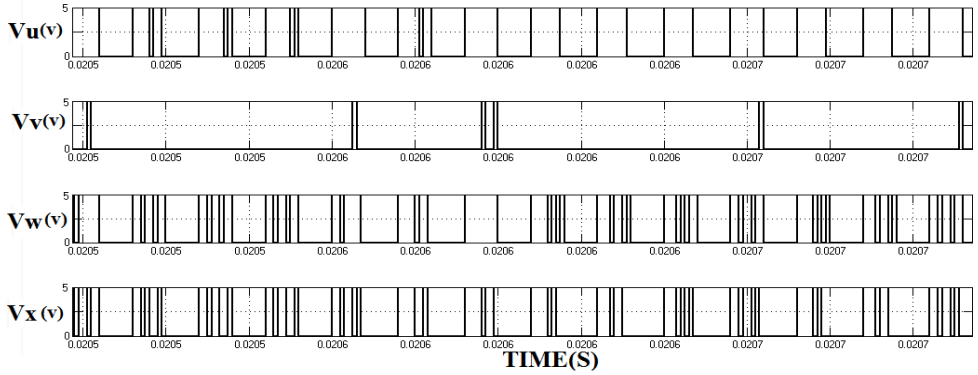

Fig. 3 Gate signals of switches s_u, s_v, s_w and s_x.

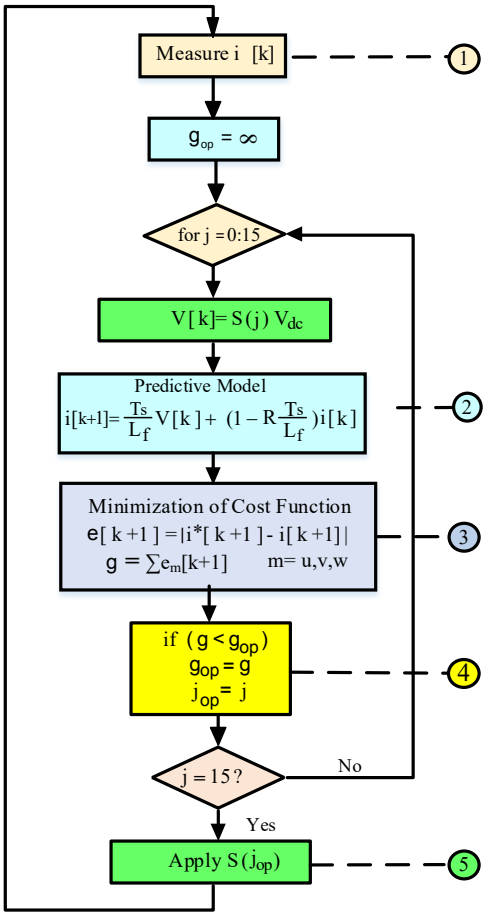

Fig. 4 FS-MPC flowchart for current control in a three-phase inverter.

Table 1 Inverter circuit details.

Parameter	Description	Value
V_{dc}	Input DC voltage	140 v
f	Load frequency	50Hz
R_u	Load resistance	5 Ω
R_v	Load resistance	3.5 Ω
R_w	Load resistance	4 Ω
R_x	Load resistance	5 Ω
$R_{fu}= R_{fv}= R_{fw}= R_{fx}$	Leakage resistance	0.05Ω
$L_{fu}= L_{fv}= L_{fw}= L_{fx}$	Leakage inductance	6 mH

As the studied inverter has 16 different switching combinations, predicted currents (8) and cost function (10) are calculated 16 times during every sampling period. So, depending on the sampling frequency and the speed of the controller, the sampling period of the load currents and the switching period can be noticeable. If the computation time is greater than the sampling period, the load current will oscillate around its reference and leads to increasing the current ripple [14]. The computation time depended on the number of functional units, word length, and controller clock. Two arithmetic structures (scheduling) of digital architecture for fixed-point computing of cost function are depicted in Fig. 6. In this figure, a, b and c are coefficients of Eq. (8).

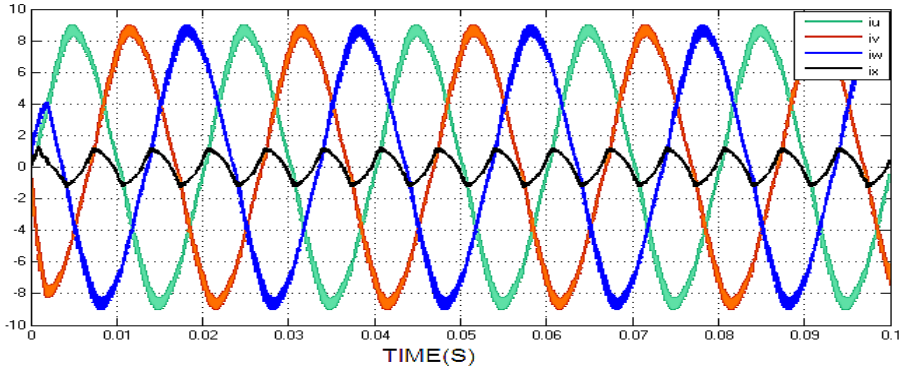

Fig. 5 Load current under unbalanced load condition.

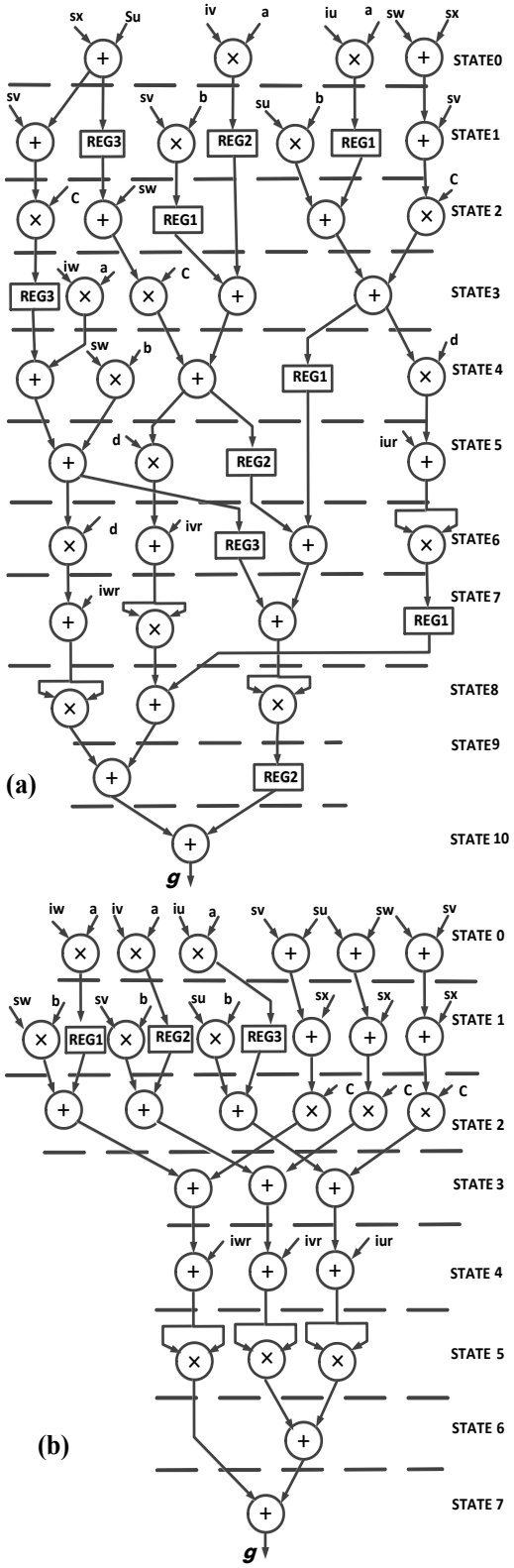

Fig. 6 Arithmetic structure for the computing cost function. (a) with 4 functional units. (b) with 6 functional units.

In Fig. 6(a), there are four functional units (two adders and two multipliers). So for computing cost function, there are eleven states. In Fig. 6(b), there are six functional units (three adders and three multipliers) and eight states. Approximately the calculation time (number of clock cycles) of each state is equal to word length. We have found a formula for calculating the number of needed Clock Cycles (CC) in each sampling instant. This formula is:

$$CC = 2^n \times N \times WL \tag{11}$$

Where n is the number of switches, N is the number of states, and WL is word length. By computing CC we can estimate the calculation time for each sample. This number effect on complexity and cost of digital controller.

5 Result

Two fixed point architectures mentioned in the previous portion are coded in VHDL and synthesized on an Altera Cyclone-IV FPGA board. To show the sampling frequency effect on the cost of digital architecture, two following cases are considered.

5.1 Clock Frequency=100 MHz and WL=32 bits

In this case, according to Eq. (11), the number of clock cycles for Fig. 6(a) is 5632 (16×11×32). This number for Fig. 6(b) is 4096. So, the needed time to calculate the cost function for all switching combinations in Fig. 6(a) and Fig. 6(b) are 56.32 µs and 40.96 µs respectively. As a result, the maximum sampling frequency ($f_{s,max}$) in this case for Fig. 6(a) is 17.75 kHz and for Fig. 6(b) is 24.41 kHz. Output current and FFT analysis for phase u in sampling frequency 17 kHz and 24 kHz is depicted in Fig. 7. For f_s=17 kHz the THD of i_u is 3.2% and for f_s=24 kHz the THD equal to 1.4%. The area that the controller has used in the FPGA board is present in terms of the number of slices. In Fig. 6(a) the number of slices is 181 and in Fig. 6(b) this number is 273.

5.2 Clock Frequency=100 MHz and WL=8 bits

In this state, the number of clock cycles for Fig. 6(a) is 1408, and for Fig. 6(b) is 1024. Therefore, the maximum sampling frequency for Fig. 6(a) and Fig. 6(b) are 71.02 kHz and 97.65 kHz respectively. The output current and FFT analysis are similar to Fig .7. For f_s=70 kHz the THD of i_u is 5.2% and for f_s=95 kHz the THD equal to 3.4%. In this state for architecture in Fig. 6(a), the number of slices is 181 and in Fig. 6(b) this number is 273.

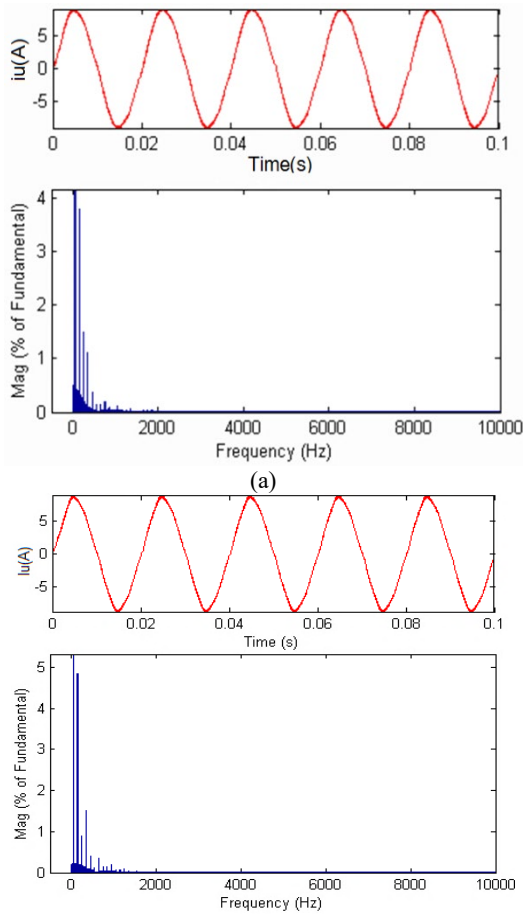

Fig. 7 Output current for phase u. (a) WL=32, f_s=17 kHz (b) WL=32, f_s=24 kHz.

In Table 2, the results for other cases are represented.

According to these results, there are relations between sampling frequency and implementation cost. By increasing sampling frequency the rate of data generation and the amount of MIPS (Million Instruction Per Second) will be increased, and we need a high processing speed, which means the number of functional units and finally, the cost of hardware will be increased. For this reason, word length must be decreased. For lower sampling frequency the number of functional units is lower and we have a lower implementation cost. In Fig. 8 these relations for WL=32bits are depicted.

6 Conclusion

The effect of sampling frequency on cost (word length and number of functional units) of FPGA-based digital controller in predictive control of three-phase inverter is verified. By knowing the number of clock cycles in each sample, the relationship between cost and hardware complexity with the sampling frequency can be determined. We have considered two fixed-point arithmetic structures with four and six functional units. In a structure with four functional units, the maximum sampling frequency is 71 kHz for WL=8 bits and 17.7 kHz for WL=32 bits. In other structures, the maximum sampling frequencies are 97.6 and 24.4 kHz for WL=8 and WL=32 bits respectively. Therefore by the increasing sampling frequency, the number of functional units (area on board and number of slices) will be increased; consequently, the implementation cost of the digital controller will be increased.

Table 2 Results for various cases with clock frequency = 100 MHz

	Fig. 5(a)				Fig. 5(b)			
WL	8	16	24	32	8	16	24	32
f_{smax} (KHz)	71	35.5	23.6	17.7	97.6	48.8	32.5	24.4
slices	49	95	138	181	74	143	208	273
THD%	5.2	4.5	3.9	3.2	3.4	2.8	2.1	1.4

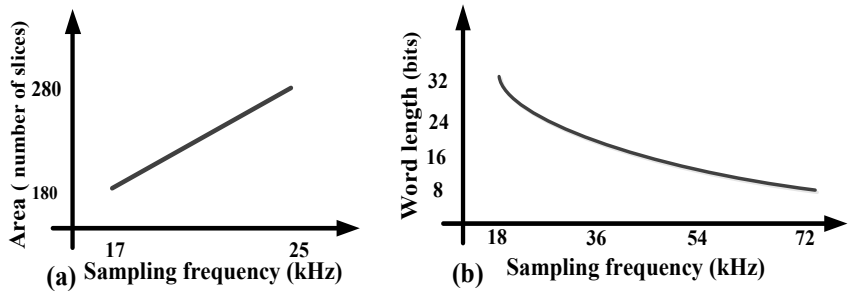

Fig. 8 Effect of sampling frequency on the cost of digital architecture.
(a) Effect on the area for WL=32bits.
(b) Effect on word length for architecture in Fig 5a.

Intellectual Property

The authors confirm that they have given due consideration to the protection of intellectual property associated with this work and that there are no impediments to publication, including the timing to publication, with respect to intellectual property.

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Credit Authorship Contribution Statement

A. Hamidi: Idea & Conceptualization, Research & Investigation, Data Curation. **S. Karimi:** Software and Simulation, Analysis. **A. Ahmadi:** Supervision, Revise & Editing.

Declaration of Competing Interest

The authors hereby confirm that the submitted manuscript is an original work and has not been published so far, is not under consideration for publication by any other journal and will not be submitted to any other journal until the decision will be made by this journal. All authors have approved the manuscript and agree with its submission to "Iranian Journal of Electrical and Electronic Engineering".

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