

## Technical Note

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# Fault Tolerant and Congestion-Aware Routing Algorithm in a Partially Connected 3D Network on Chip

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## Abstract

Electronic Control Units (ECUs) play an important role in the system of vehicle. Network-on-Chips (NoCs) also have been accepted as a standard communication platform in many-core systems. However, they possess high network latency and consume large power. In this paper, we present a standard Network-on-Chip platform compatible for a centralized ECU to avoid loss of related function. We introduce a minimal routing algorithm in partially connected 3D Network-on-Chip, in which a fixed place of Through Silicon Vias (TSVs) is designed to reduce TSV implementation cost which can be provided as a standard in the automotive electronics industry. This routing algorithm employs network congestion and fault information (network metrics) to find the minimum path while avoiding traversing the faulty paths. The proposed algorithm consists of in-layer routing and interlayer routing. The intra-layer routing algorithm employs an information propagation network to propagate control information between nodes located in the same layer. It uses a parameter called index to select the optimum path between nodes in the same layer. The index value is updated periodically based on a faulty link or a faulty node and published across networks. The interlayer routing algorithm is performed based on the minimum path to the elevator routers. The proposed algorithm reduces the average packet latency and increases the network throughput. The simulation results indicate that our routing algorithm improves network latency by 15.3% compared to two other routing algorithms.

**Keywords** Fault-tolerant; Congestion-aware; Index Mechanism; 3D-NoC; routing; Centralized ECU

## Introduction

Designing a vehicle, which lowers battery usage is so important [1]. So, implementing a standard platform and low power component plays a critical role in this technology. A centralized Electronic Control Unit (ECU) approach can avoid malfunction generated by ECU faults. In this structure, each ECU can communicate with any sensor. We present a Network-on-Chip (NoC) platform that is suitable for a centralized ECU to avoid fault in communication. Network on Chips present an interconnection platform for high-performance communication

in a many-core system [2-4]. As technology scales, the integration of a large number of blocks and cores on a chip increases network latency and power consumption. Three-dimensional (3D) NoC provides a viable solution to reduce the network latency by decreasing the number of hops between the blocks [5, 6]. Multi-layers of 2D NoC are connected using Through Silicon Vias (TSV's). TSVs provide faster and better communication between layers in terms of energy consumption. However, 3D NoCs face some challenges including high power consumption, thermal issue, and implementation cost. A different solu-



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tion including router architecture and routing algorithm has been presented to address these challenges [7-9]. The routing algorithm has an important effect on the 3D NoC performance [10].

In [7], the supply voltage is reduced to save power consumption at the cost of network congestion and latency increment. In [8], the routing computing is performed based on the estimated temperature of routers in each cycle. 3D routers propagate an index that is dynamically updated to notate the temperature of the routers. This approach leads to receiving fewer high temperature packets by the 3D router.

TSVs implementation cost imposes high overhead in 3D NoCs. Therefore, partially connected 3D architectures are presented to reduce this cost [11-13]. In partially connected 3D NOCs, only some routers in one layer have vertical links (elevators). Therefore, elevators are used as a communication interface between the exposed layers. In this case, some routers are heavily loaded, while others may be idle, which causes congestion in some regions. Therefore, the allocation of elevators is critical to network performance.

The authors in [12] present a partially connected NF-IC-based 3D NoC to increase the robustness and fault creation. The partially connected 3D NoC introduced in [13] aims to improve congestion and traffic distribution. In [6], a partially connected 3D NOC is presented, which uses an indexing mechanism in the routing procedure to find the most appropriate TSV. However, it does not change the index value based on the different network statuses.

In [14], a routing algorithm for partially connected 3D-NoCs is introduced that tolerates the faults on links by employing intermediate routers. However, it cannot outperform the performance compared to the non-adaptive routing algorithms.

On the other hand, the reliability issue demands an effective solution to avoid packet transmission from horizontal/vertical faulty links, and links including soft errors or crosstalk. In this paper, the proposed routing algorithm presents a mechanism for updating and propagating traffic information to prevent regional congestion. It also avoids packet transmission along faulty paths.

The paper is organized as follows. We review the related works in Section II. The propagation and updating procedure of the index value is discussed in Section III. In Section IV, our routing algorithm is explained. The simulation results and analysis are investigated in section V. Then, we concluded the paper in section VI.

## RELATED WORK

NoC as an acceptable communication infrastructure pro-

vides high performance in many-core systems. 2D NoCs possess high latency by integration of many cores on a chip. Also, the large volume of data demands high resource utilization that leads to high power consumption and network congestion. Three-dimensional NoCs present higher performance compared to 2D NoCs by reducing the distance between nodes. A 3D NoCs connect multi-layers of 2D NoCs using TSV's, together. Therefore, packet transmission latency is reduced due to a reduction in the distance between cores. However, 3D NoCs impose high power consumption due to the high power of routers [15]. Also, they possess a large overhead due to the high implementation cost of TSVs. Reconfigurable circuit tries to reduce high power consumption [16-18]. The author in [18] try to change the supply voltage level based on the error tolerance of an application. However, the voltage scaling technique increases network congestion, latency and output error.

Many routing algorithms have been presented to tolerate faults [19-21]. In [19], a fault-tolerant routing algorithm is proposed in 3D NoCs, which connects different layers, heterogeneously. It relies on a virtual channel to avoid deadlocks and tolerates multiple faults in vertical links. However, a large number of TSVs leads to high implementation costs. In [20], a fault-tolerant algorithm is introduced in which a table and two TSV status vectors are used in each layer instead of global Routing. These vectors are used for the fault status of links. The main problem of this algorithm is using the table which imposes a lot of hardware overhead and prevents scalability. A partially connected 3D NOC is introduced in [6] that finds the optimum TSV by employing an indexing mechanism. However, it does not change the index value based on the different network statuses.

In the CDA routing algorithm [21], a dynamic elevator allocation mechanism is proposed that considers both distance and network congestion information. It selects the elevator based on the existing path from the source router to the elevator. It connects the layer in a partial manner of 3D NoC. Therefore, the network delay is considerably reduced. However, it does not employ faulty links information and may face with blocked path.

We propose a partially connected 3D NoC that has a limited number of TSV's. We provide a routing algorithm that improves NoC performance by being aware of network congestion and fault. The proposed algorithm can reduce network latency by preventing packet transmission along faulty and congested paths.

## THE PROPAGATION AND UPDATING PROCEDURE OF THE INDEX VALUE

In this section, the details of the propagation and updat-

ing of the index value in the proposed algorithm are explained. In order to send information about the elevator existence to other routers, an index propagation structure is required, in which a parameter called index is used. The index parameter indicates the distance between the current router and the elevator router. The higher value of this parameter indicates the shorter distance between the current router and the elevator node. The index value is set to an initial value based on the dimensions of the NoC, and its value would be reduced by one after passing each router.

In order to be aware of faulty routers, if a node is adjacent to a node with a bug, we set its index value to zero when updating and sending it to neighbouring routers. Therefore, this mechanism reduces the selection possibility of the path that includes faulty routers. Each router receives different values of the index from the four directions of north, east, south and west, so it must have 4 registers for corresponding directions in the current router (Fig. 1). To propagate the value of the index to neighbour routers, each node selects the largest index after receiving all indexes. Then, it would be reduced by one unit for transmission to all output directions. Fig. 2 shows the initialization steps of the indexes.

First, all index values are equal to zero and the elevator routers reduce the value of the initial index 6 (one unit) after initializing the indexes (in the mesh network with six rows and six columns, and sending it to neighbouring routers. If there is no neighbour next to the elevator router, its index value will be considered zero. After propagation of index values in the network, all routers are aware of their distance to the elevator routers, and the larger value of the index means the shorter distance to the relevant elevator router.

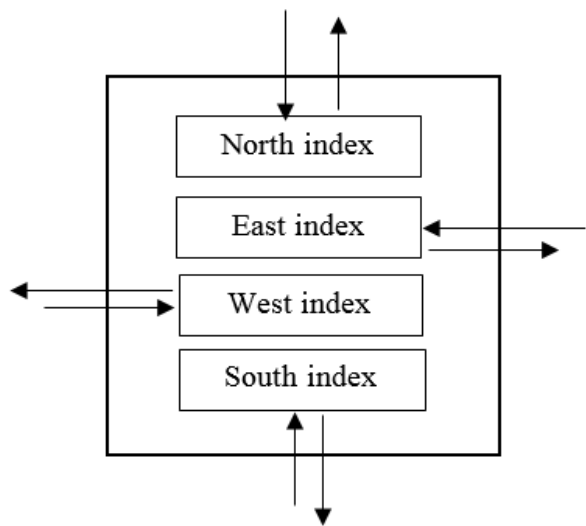


Fig 1. The structure of the indexes registering.

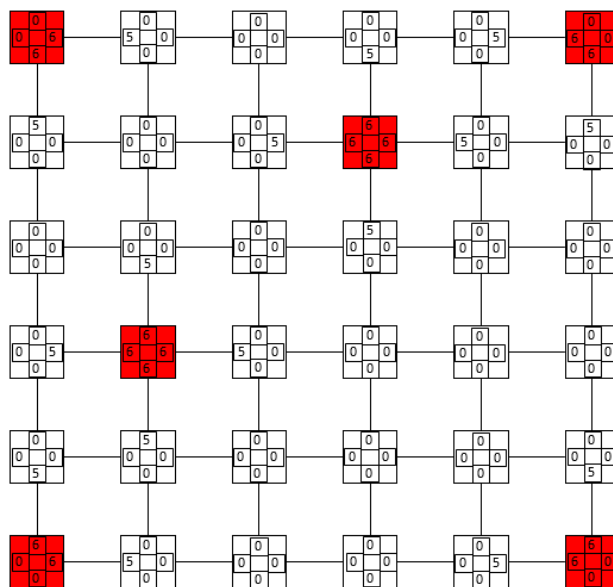


Fig 1. The first step of the index propagation in the proposed method.

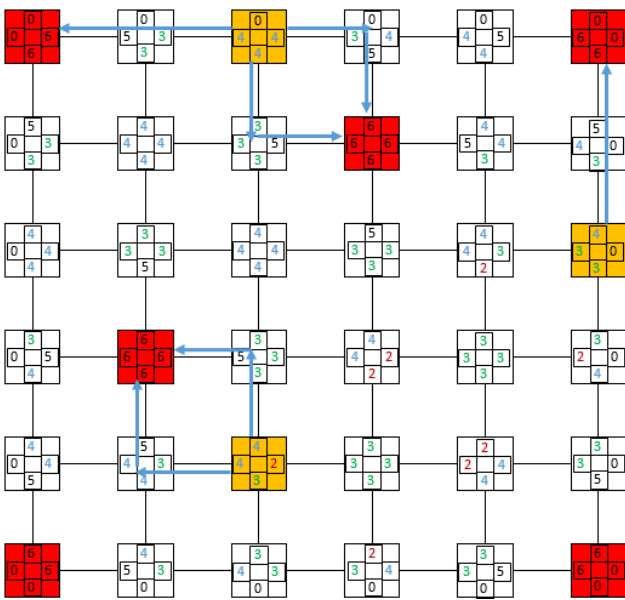
**THE PROPOSED ALGORITHM**

Our proposed routing algorithm is summarized in algorithm 1. An example is shown in Fig. 3 that illustrates how to select an elevator router in the proposed method. The orange squares in this example are ordinary routers that are supposed to determine their path to the elevator routers (red squares) due to the index values. Blue paths are different possible paths that can be used to reach elevator nodes.

In the proposed method, to provide a fault-tolerant routing algorithm at the existence of a faulty node or a faulty link, the adjacent nodes would set the value of the indexes to zero so that other nodes are aware of the cross-failure signals in the network. When adjacent nodes with this node want to send their packets in the network, they would not send it to the relevant direction due to receiving the zero index from this neighbour. Therefore, the algorithm would be aware of the existence of a faulty node or a faulty link in the network, which prevents these paths from data transmission.

```

Algorithm 1: Routing Algorithm
Proposed_Routing_Algorithm (input: current,destination,index_in|
    output:best_direction) {
01: if (current router and destination route are not in the same layer)
02:   best_direction = External_Routing_Algorithm
    (current,destination)
03: else
04:   best_direction = Internal_Routing_Algorithm
    (current,destination,index_in)
05:;}
    
```



**Fig 2.** An example of the path selection to those routers which have elevator.

The intra-layer routing algorithm is depicted in algorithm 2. As the inputs, all available output directions and index values and the number of empty houses are received, and the best output direction is sent as the output (best\_direction). In interlayer routing, the best elevator router is selected based on the parameters of distance, density and error, in which the minimum distance to the elevator router is considered.

**THE RESULT AND ANALYSYS**

In this section, to evaluate the proposed algorithm, the simulation environment and the evaluated parameters are examined. Then, the simulation results are evaluated and analyzed. Our routing algorithm is simulated by the access Access-Noxim simulator for seven TSVs and twelve TSVs.

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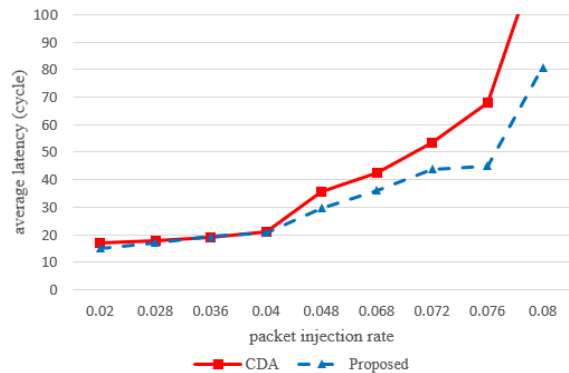
Algorithm 2: Intermediate Routing Algorithm
01: Internal_Routing_Algorithm (input: all_directions, Index [ ],
buffer_empty [ ])
02:                               output: best_direction) {
03: best_directions []: to store all available best directions to the
destination
04:
05: // select best output according to the index and buffer
06:   for each di in in all_directions [ ] {
07:     best_directions [ ] = Max (Index [di] + (buffer_empty
[di] 2)
08:   }
09: // if there are more than one direction then select one as
random
10: best direction = Random (best_directions [ ])
11: ;}
    
```

The details of the simulation parameter of the proposed routing algorithm are summarized in Table I. Based on the placement of TSV nodes and faulty nodes, different simulations have been performed and repeated for different traffic patterns.

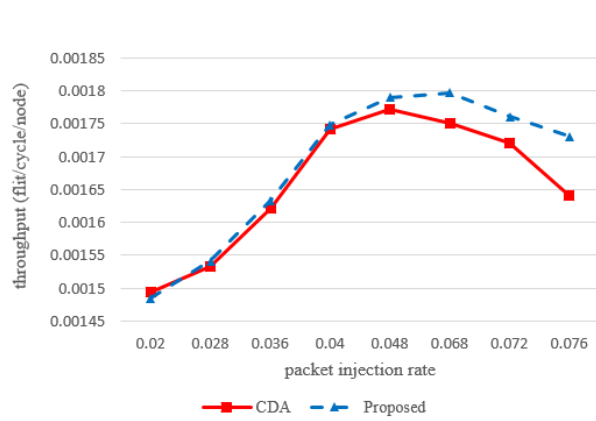
Fig. 4 and Fig. 5 Show the average packet latency for different algorithms in Uniform and Transpose traffic patterns for 7 TSVs, respectively.

**Table 1.** Simulation setup

Simulator	Access Noxim
Network Size	7×7×4
Traffic Simulation	50000 Cycles
Buffer depth	4 flits
Packet Size	8 flits
Traffic Pattern	Random: Uniform and Transpose



**Fig 3.** The packets latency for uniform traffic with 7 TSVs.



**Fig 4.** The network throughput for uniform traffic with 7 TSVs.

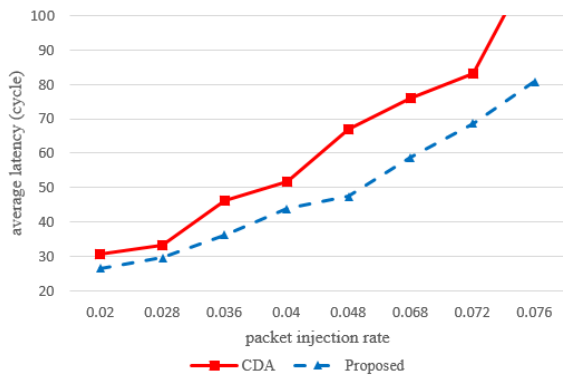


Fig 5. The packets latency for transpose traffic with 7 TSVs.

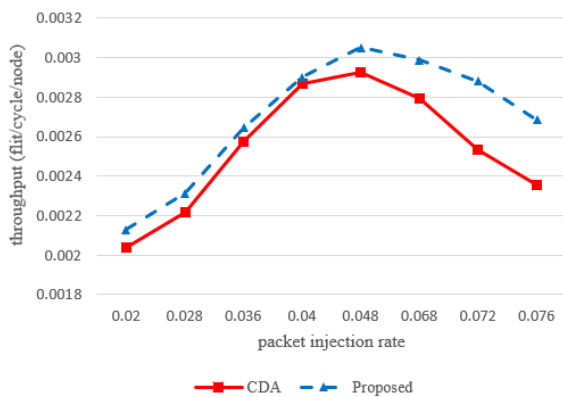


Fig 6. The packets latency rate for uniform traffic with 12 TSVs.

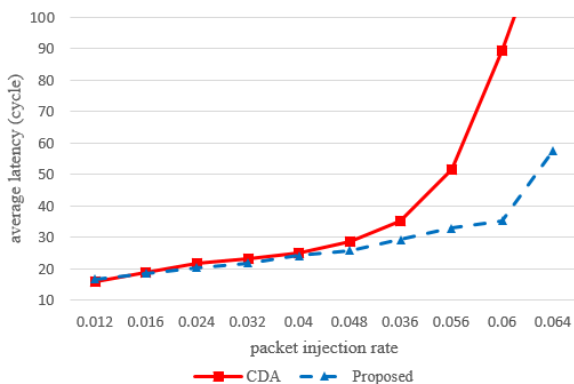


Fig 7. The packets latency rate for transpose traffic with 12 TSVs.

The proposed algorithm outperforms the CDA algorithm in average packet latency by 20% and 10.6% for Uniform and Transpose traffic, respectively. In the Transpose traffic pattern, the proposed algorithm has lower average

latency at higher injection rates. Also, Fig. 6 and Fig. 7 Show network throughput for mentioned algorithms in different traffic patterns. As the figures indicate, the proposed algorithm provides higher network throughput compared to the CDA algorithm by 10.8% and 25% for Uniform and Transpose traffic, respectively. We repeat the simulation results for twelve TSVs. Fig. 8 to Fig. 11 indicate that by increasing the number of TSVs, the network latency and throughput are improved. This is due to the more path existence when the number of TSVs increases. Therefore, our proposed algorithm improves network latency and throughput while reducing TSVs implementation overhead, significantly. Our routing algorithm avoids employing faulty paths due to knowing a faulty node or a faulty link in the network.

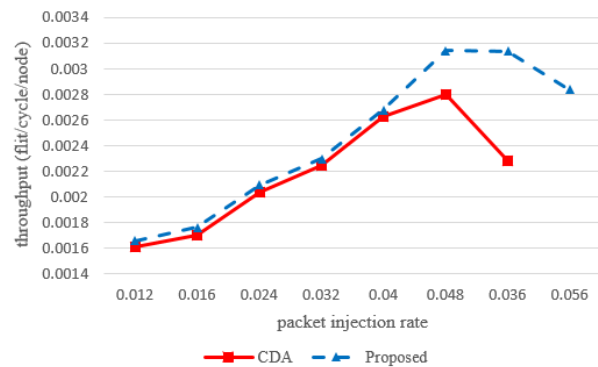


Fig 8. The network throughput for uniform traffic with 12 TSVs.

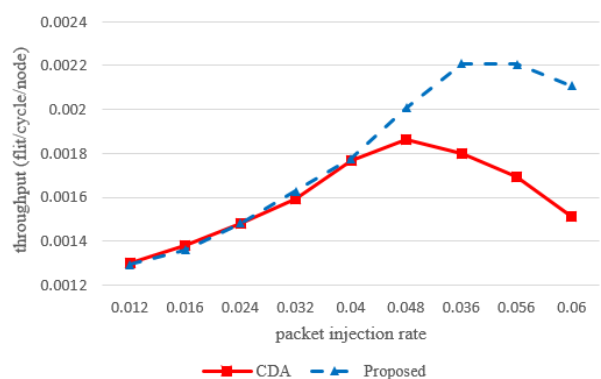


Fig 9. The network throughput for transpose traffic with 12 TSVs.

### CONCLUSION

Compilation of standards and design of low power components in vehicle technology plays an important role. NoCs as a promisable platform in communicating high

performance component is considered in the proposed paper. In this paper, we present a standard Network-on-Chip platform compatible for a centralized ECU to avoid loss of related function. We introduce a partially connected 3D Network-on-Chip. We employ a fixed number of TSVs that are already placed based on the type of application and the relevant traffic pattern to reduce TSV implementation costs. We present a routing algorithm that improves network performance by employing network congestion and fault information. The proposed algorithm finds the optimum path based on minimum distance and avoids traversing faulty paths. Our routing algorithm consists of two parts: in-layer routing and interlayer routing. The proposed intra-layer routing algorithm is used to transfer control information between nodes located in the same layer. To implement this part of the routing algorithm, an in-layer information propagation network is used and the routers use a parameter called index to select the optimum path between nodes in the same layer. The index value is updated periodically based on a specific fault-tolerant algorithm and published across networks. The interlayer routing algorithm is also used to transfer information between different layers of the network based on the minimum path to the elevator routers. The proposed algorithm outperforms the other algorithms by reducing the average packet latency and increasing the network throughput.

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### Declarations

#### Ethics approval and consent to participate

Not applicable.

#### Consent for publication

Not applicable.

#### Competing interests

The authors declare that they have no competing interests.

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