Voltage Control of Three Phase Inverters by Using Active Disturbance Rejection Control

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Abstract

Control of three phase inverters has been an important issue in recent years. This paper proposes active disturbance rejection control (ADRC) scheme for controlling three phase inverters. The main advantage of ADRC that motivated us for using this controller for inverter is that it is model independent. This controller is used in a double loop structure including an inner current loop and outer voltage loop. A case study has been simulated in SIMULINK to demonstrate the advantages of ADRC in control of inverters over PI controller. Simulation results demonstrate that load changes have no impact on performance of this control method and it is not sensitive to any uncertainty in parameters of the inverter.

Keywords: Component; Active disturbance rejection control (ADRC); Three phase inverter; Voltage control.

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1. Introduction

Nowadays, three phase inverters are widely used in diverse applications such as uninterruptible power systems (UPS's) and integration of distributed generations (DG's) [1]. Control of three-phase inverters is a major challenge to many engineers [2]. In UPS applications, it is crucial to regulate the output voltage for different load conditions [3].

In most of industrial applications, PID controllers are implemented for controlling three phase inverters. PID controller is mainly used in a double loop control structure in order to enhance system performance [4]. The inner loop includes a PID controller for regulating the current. Moreover, another PID controller is used in outer loop such that the voltage of the inverter tracks the reference by a predefined specific dynamic characteristic [5]. This control method is implemented through the gating signals generated by using pulse width modulation (PWM) technique.

By advent of digital signal processors (DSP's), it was the best time to implement more sophisticated control schemes. Dead beat control [6], [7], [8], sliding mode control [9], [10], robust control [11], [12], [13]and predictive control [14]are the most important schemes that have been used for controlling three phase inverters. Although the aforementioned control methods have satisfactory results, the PID controllers are prevalent nowadays. This is mainly due to the fact that PID controllers are simple and convenient. In industrial applications, there are uncertainties in parameters of the model for which approximate estimations are provided which are not accurate enough [15]. Therefore, using a control approach that is not model based is critical.

In this paper, this issue is addressed by proposing a new control method known as Active Disturbance Rejection Control (ADRC). The main advantage of this method is that it is model independent [16], [17]. This feature is the result of exploiting a state observer that estimates the disturbances and the controller actively rejects them [17]. The purpose of this research is to use this new control method for voltage control of three phase inverter in UPS applications. This is accomplished by using a double loop structure control including

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an inner current loop and also outer voltage loop control.

The proceeding parts of this paper are classified as follow: in section II, ADRC is overviewed. In section III, at first the three phase inverter is modeled. After that, structure of ADRC for the inverter is discussed. In section IV, a case study is used to simulate the performance of ADRC and compare its results with PI controller. Finally, section V includes the conclusion of this paper.

1. Active disturbance rejection control (ADRC)

As shown in Fig. 1, the structure of ADRC contains an observer and a controller part. Observer is used to estimates the disturbance and states of the system. The outputs of the observer are used by a control law in order that the disturbances can be rejected. Accordingly, the output can track the reference with a predefined dynamic characteristic. In this paper, the idea of ADRC is explained for a second order plant. Ref [18] provides more information about ADRC.

Consider a second order plant with the form of

$$\ddot{y} = a_1\dot{y} + a_2 y + d + bu \tag{1}$$

where, y is the output, u is the input of the system and d is the external disturbance. If b_0 is supposed to be the estimated value of , then (1) can be rewritten as

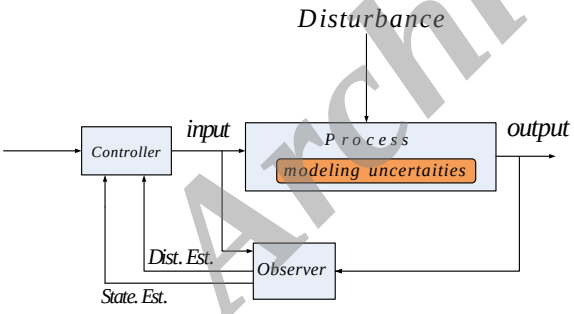

Fig. 1. Simplified block diagram of ADRC for a process

$$\ddot{y} = a_1\dot{y} + a_2 y + d + (b - b_0)u + b_0 u = f\left(t, y, \dot{y}, \omega\right) + b_0 u \tag{2}$$

here, $f\left(t, y, \dot{y}, d\right)$ or briefly f is known as *general disturbance*. If the general disturbance is estimated and cancelled the system is reduced to a double-integral system. This is done by employing a control law which is defined as

$$u = \frac{u_0 - f}{b_0} \tag{3}$$

By replacing (3) in (2), the simplified model of the system is deduced as

$$\ddot{y} = u_0 \tag{4}$$

Now the control problem is reduced to designing a controller for a system described by (4).

It is sufficient to control the reduced model by using a corrected PD controller as indicated in Fig. 2 [19]. With regard to (4) and Fig. 2, the transfer function of reference to output is as,

$$\frac{y(s)}{y_{ref}(s)} = \frac{K_p}{s^2 + K_D s + K_p} \tag{5}$$

where, K_p and K_D are the parameters that should be tuned. For simplicity of tuning, K_p and K_D are selected such that both poles of the transfer function will be located at $-\omega_c$ [20]. In other words,

$$\frac{y(s)}{y_{ref}(s)} = \frac{\omega_c^2}{s^2 + 2\omega_c s + \omega_c^2} = \frac{\omega_c^2}{(s + \omega_c)^2} \tag{6}$$

Therefore, $K_p = \omega_c^2$ and $K_D = 2\omega_c$ and ω_c is known as the bandwidth of the controller.

As indicated in Fig. 2, for eliminating the effect of disturbance, the general disturbance (f) and the state space of the system must be estimated. This is accomplished by using an extended state observer (*ESO*).

The state space equations of *ESO* is defined as [19]:

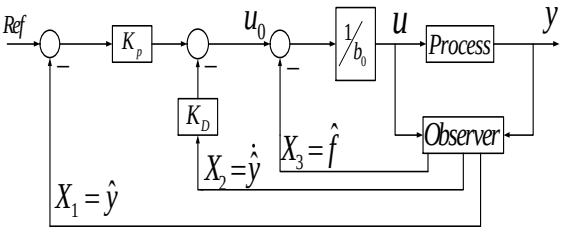

Fig. 2. Control structure of ADRC for a second order system

$$\begin{pmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{pmatrix} . \begin{pmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{pmatrix} + \begin{pmatrix} 0 \\ b_0 \\ 0 \end{pmatrix} u(t) + \begin{pmatrix} l_1 \\ l_2 \\ l_3 \end{pmatrix} . \left(y(t) - x_1\right) \tag{7}$$

where, $L = \begin{bmatrix} l_1 & l_2 & l_3 \end{bmatrix}$ is the observer gain vector and x_1, x_2 and x_3 are estimated values of $y, \dot{y}$ and f respectively. According to (7), the characteristic polynomial of the observer is as,

$$\gamma(s) = s^3 + l_1 s^2 + l_2 s + l_3 \tag{8}$$

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For simplicity of tuning, the elements of the observer gain vector are chosen such that all the eigenvalues of the observer are located at $-\omega_o$ [19]. Therefore, the characteristic polynomial of the observe can be defined as follows,

$$\gamma(s) = s^3 + l_1 s^2 + l_2 s + l_3 = (s + \omega_o)^3 \quad (9)$$

Regarding (9), l_1, l_2 and l_3 (the observer gain vector) can be calculated. It's worth mentioning that ω_o is the bandwidth of the observer. Therefore, in ADRC there are only controller and observer bandwidths that should be tuned. Thereafter, other parameters of ADRC can be calculated.

2. Modeling and control of three phase inverter by using ADRC

Consider Fig. 3 which shows an inverter with output *LC* filter which is connected to a parallel *RLC* load. In this figure, V_t and V_s are terminal and load voltages respectively. L_t and R_t are inductance and resistance of the inductor. C_f represents the capacitance of the capacitor bank and i is the inductor current. The inductor current equation is derived as,

$$L_t \frac{di}{dt} = V_t - V_s - (R_t + r_{on})i \quad (10)$$

where, r_{on} is the resistance of the inverter switch. By transforming to dq-frame, (10) can be rewritten as:

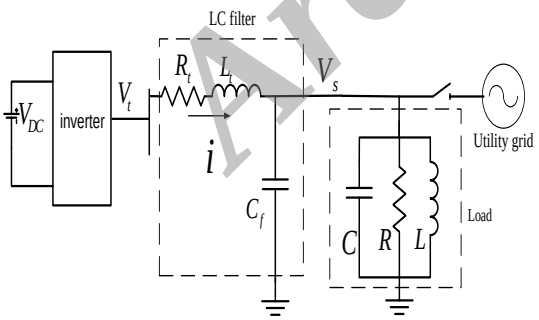

Fig. 3. Three phase inverter with an output LC filter

$$L \frac{di_d}{dt} = L\omega i_q - (R + r_{on})i_d + V_{td} - V_{sd} \quad (11)$$

$$L \frac{di_q}{dt} = -L\omega i_d - (R + r_{on})i_q + V_{tq} - V_{sq} \quad (12)$$

where, ω is the angular frequency of the system and d and q indices depict the values of parameters in d and q axes respectively.

Based on average model of the inverter proposed in [21], V_{td} and V_{tq} are

$$V_{td}(t) = \frac{V_{DC}}{2} m_d(t) \quad (13)$$

$$V_{tq}(t) = \frac{V_{DC}}{2} m_q(t) \quad (14)$$

here, m_d and m_q are the inverter modulation signals. Due to the presence of $L\omega$ terms in (10) and (11), dynamics of i_d and i_q are coupled. To decouple the dynamics, m_d and m_q are defined as

$$m_d = \frac{2}{V_{DC}}(u_d - L\omega i_q + V_{sd}) \quad (15)$$

$$m_q = \frac{2}{V_{DC}}(u_q + L\omega i_d + V_{sq}) \quad (16)$$

where, u_d and u_q are two new control input signals. Substituting for m_d and m_q in (11) and (12), respectively, from (15) and (16) and also using (13) and (14) for V_{td} and V_{tq} respectively, the following equations can be deduced as,

$$L \frac{di_d}{dt} = -(R + r_{on})i_d + u_d \quad (17)$$

$$L \frac{di_q}{dt} = -(R + r_{on})i_q + u_q \quad (18)$$

Accordingly, (17) and (18) describe the inverter current dynamics in dq frame. The control inputs (u_d and u_q) should be adjusted in order that the inner current loop can be used to regulate the current. These control inputs are the outputs of ADRC. In the next subsection designing the ADRC for the inner current loop will be introduced.

A) Designing ADRC for Current Loop

Equations (17) and (18) describe two decoupled, first-order, linear systems. Based on (17) and (18), i_d and i_q can be controlled by u_d

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and u_q, respectively. Fig. 4 shows a block representation of the d- and q-axis current controllers of the inverter in which u_d and u_q are the outputs of two corresponding controllers.

The simplified block diagram of Fig.4 is shown in Fig.5. In this figure, $b_0 = \frac{1}{L}$ and K_p can be adjusted such that the equivalent transfer function for the current loop is as

$$G_i(s) = \frac{1}{\frac{1}{K_p}s + 1} = \frac{1}{\tau_i s + 1} \quad (19)$$

where, τ_i is the time constant of equivalent system of current loop. Hence, tuning of K_p and τ_i are identical.

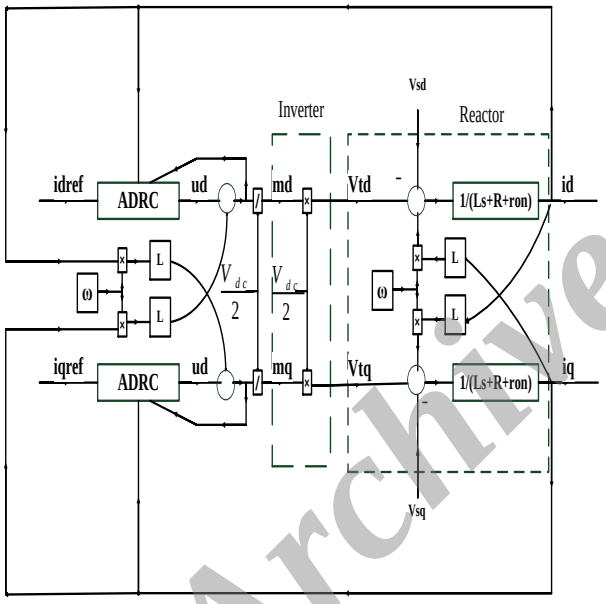

Fig. 4. Current loop structure of ADRC in dq-frame

B) Designing ADRC for Voltage Loop

Referring to Fig. 3, dynamics of the load voltage are as:

$$C_f \frac{dV_s}{dt} = i - i_L \quad (20)$$

By using *dq*-transformation for (20), the equations in dq-frame are as,

$$C_f \frac{dV_{sd}}{dt} = C_f(\omega V_{sq}) + i_d - i_{Ld} \quad (21)$$

$$C_f \frac{dV_{sq}}{dt} = -C_f(\omega V_{sd}) + i_q - i_{Lq} \quad (22)$$

Therefore, the dynamics of V_{sd} and V_{sq} are as indicated in Fig 6. Based on Fig.6, ADRC can be utilized for the outer voltage loop as shown in Fig.7. By the assumption that employing the feedforward decoupling signals have fully decoupled d and q axes, Fig. 8 can be used.

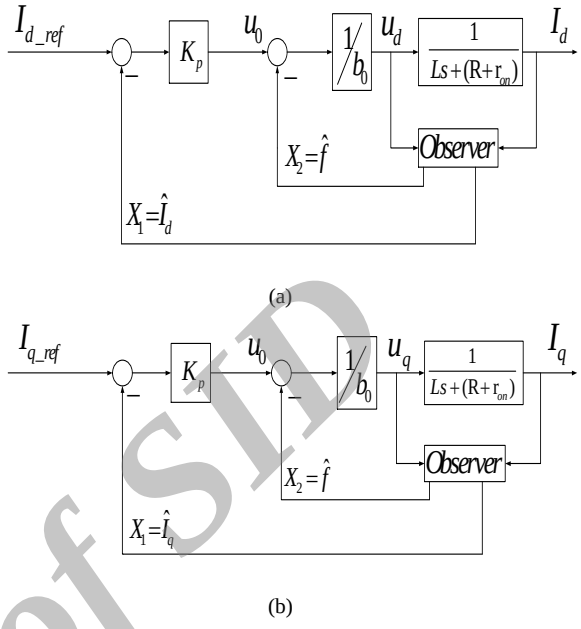

Fig. 5. Simplified block diagram of current loop of ADRC (a) d-axis (b) q-axis

In this figure, $b_0 = \frac{1}{\tau_i C_f}$ and K_p and K_D can be adjusted such that the equivalent transfer function for the current loop be as

$$G_t(s) = \frac{K_p}{s^2 + K_D s + K_p} \quad (23)$$

Therefore, by tuning the parameters the required transient response of voltage control is achievable.

3. Simulation

Simulations of the system shown in Fig. 2 are carried out by using Matlab/Simulink, to verify the proposed control strategy for a three-phase inverter. Table (1) represents the values of parameters which are used in simulation.

Designing the controller is the first step towards controlling the inverter. Based on the tuning method proposed in [22], $\omega_c = 1000 rad/s$ and $\omega_o = 4000 rad/s$. For evaluating ADRC and comparison with PI, the PI controller is also designed by using the method proposed in [21].

Suppose that at $t = 0.15s$ the reference voltage increases from $V_{s\_ref} = 400V$ to

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$V_{s\_ref} = 500V$. Then, the load with $R = 83m\Omega$ and $L = 137\mu H$ is added in $t = 0.25s$. Thereafter, at $t = 0.4s$ the reference voltage decreases from $V_{s\_ref} = 500V$ to $V_{s\_ref} = 400V$. In Fig. 9(a) the three phase voltage has been shown.

Based on dq-transformation, amplitude of the reference there phase voltage is defined as,

$$V_{s\_ref}^2 = V_{sd\_ref}^2 + V_{sq\_ref}^2 \quad (24)$$

without loss of generality, the simulation is done by the assumption that $V_{sq\_ref} = 0$. Hence, it can be concluded that $V_{s\_ref} = V_{sd\_ref}$.

As indicated in Fig. 9(b), the recovery time of ADRC is about $8ms$ while this is about $21ms$ for PI controller. Moreover, in $t = 0.4s$ the load condition has changed in comparison with $t = 0.15s$. However, the response of ADRC has not changed too much.

ADRC has the potential to eliminate load changes. Therefore, it provides an opportunity for inverter to have a sinusoidal output voltage in diverse load conditions. This is an important factor for inverters in UPS applications. This issue is studied by changing the values of RLC which are represented in Table (1).

In this simulation, the settling time (t_s) and maximum overshoot (M_o) are measured. By changing the load, their percentage deviations from their values in normal load condition are calculated. It is ideal if both of t_s and M_o don't change. However, changing the load affects these parameters inevitably. For these reasons another parameter is considered which is defined as,

$$D(\%) = \sqrt{(\Delta t_s)^2 + (\Delta M_o)^2} \quad (25)$$

where, Δt_s and ΔM_o are the percentage deviation of from their values in normal condition. Consequently, it is appropriate for the controller if *D* can be small as far as possible.

As demonstrated in Fig.10, the effect of load changes has less influence on the response of ADRC rather than PI. This is mainly due to the fact that the observer of ADRC considers the changes in load current as a disturbance and rejects it. This is a powerful aspect of ADRC; because just estimations of parameters exist in industrial applications. Therefore, it is critical for a controller to work properly if the parameters change or are not estimated accurately. The following simulation results show the response of ADRC when inductance and capacitance of the LC filter change.

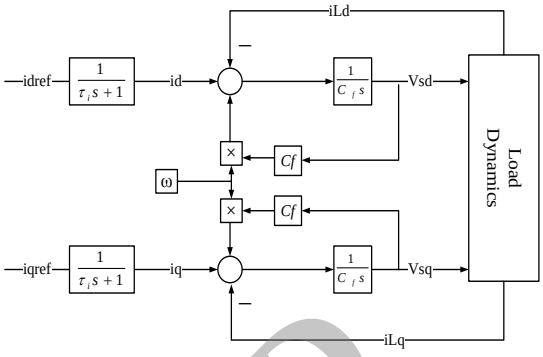

Fig. 6. Load voltage dynamics by considering equivalent system of current loop

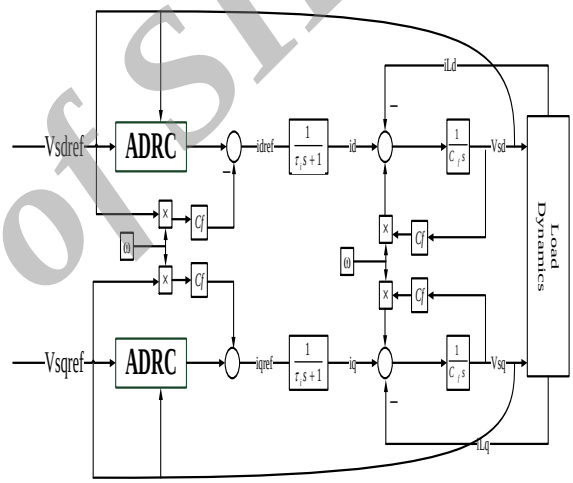

Fig. 7. Voltage loop structure of ADRC in dq-frame

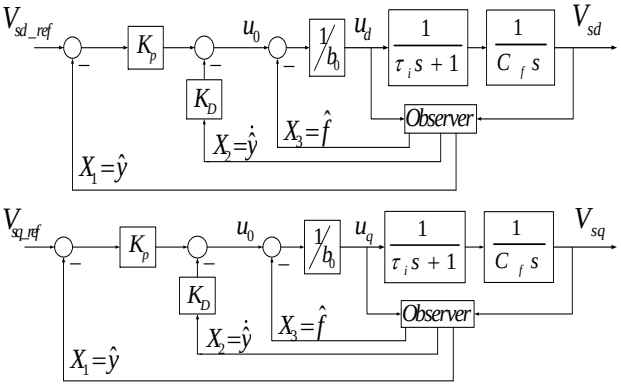

Fig. 8. Simplified block diagram of voltage loop of ADRC (a) d-axis (b) q-axis

As shown in Fig. 11(a) and Fig. 11(b), the effect of LC filter on ADRC is negligible while it severely affects the response of PI controller. Therefore, the response of ADRC is independent of parameters of the LC filter.

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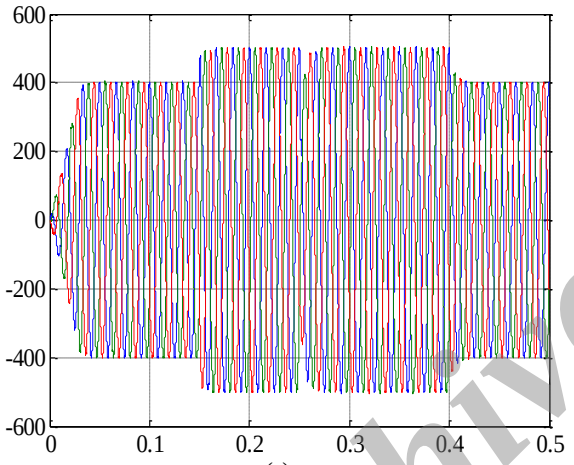
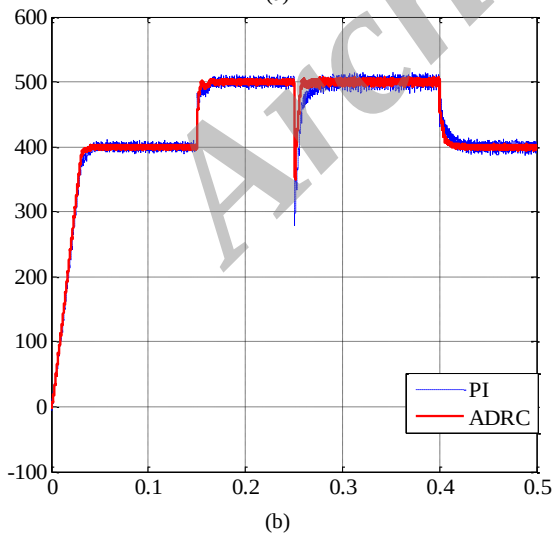
Table.1.
Parameters of the simulated system

Parameters	Physical values
R	1Ω
L	$136\mu H$
C	$27.1mF$
C_f	$2.5mF$
R_t	$1.19m\Omega$
L_t	$100\mu H$
r_{on}	$0.88m\Omega$
V_{DC}	$1500V$
Switching frequency (f_s)	$5kHz$



(a)



(b)

Fig. 9. Voltage of three phase inverter (a) three phase voltage (V_{sabc}) (b) voltage in d- axis (V_{sd})

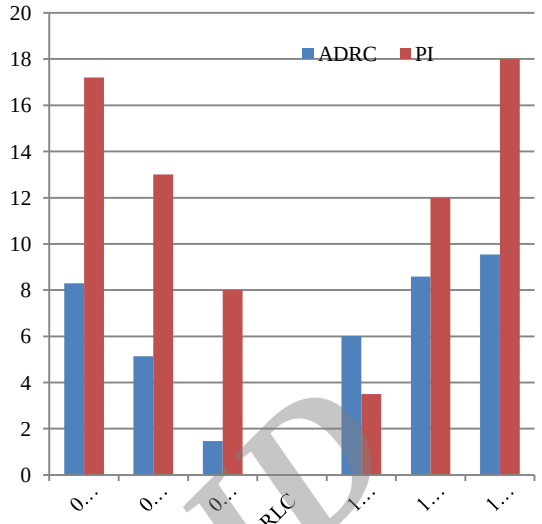
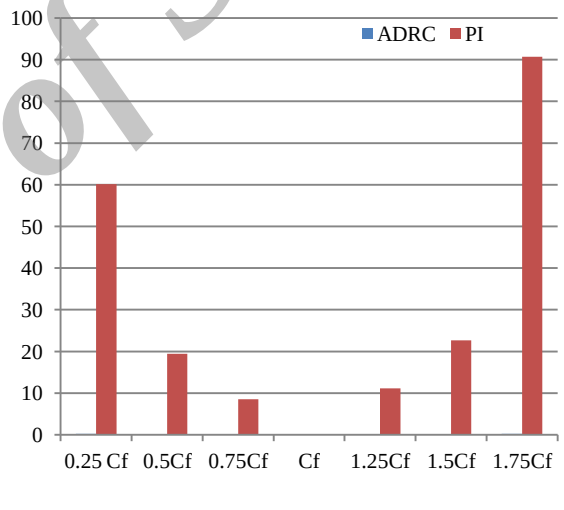
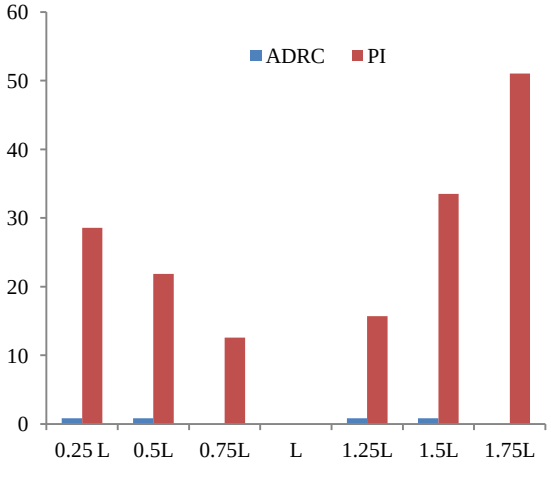


Fig. 10. Values of *D* for different values of RLC



(a)



(b)

Fig. 11. Values of *D* for different values of (a) C_f (b) L_t

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4. Conclusion

In this paper control of three phase inverters by using active disturbance rejection control (ADRC) have been investigated. At first, an overview of the idea of ADRC is conducted. Then, a detailed explanation of modeling and control of inverter by using ADRC has been provided. This is done by designing ADRC parameters for a double loop structure. In other words, ADRC is designed for inner current loop and outer voltage loop. A case study is used to confirm the advantages of ADRC over PI.

It is deduced from simulation results that changing load condition affects performance of ADRC much less than PI. Moreover, the effect of changing LC filter parameters is negligible for ADRC. This is a promising step towards enhancing performance of controllers; because there is no need to access all the detailed information about parameters. Therefore, it can be concluded that this controller can be used in the near future instead of PI controllers.

References

[1] Takao Kawabata, Takeshi Miyashita, Yushin Yamamoto, "Digital Control of Three-phase PWM Inverter with LC Filter," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 62-72, 1991.

[2] J. Rodrguez, J. Pontt, C. A. Silva, P. Correa, P. Corts, and U. Ammann, "Predictive Current Control of a Voltage Source Inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 495-503, 2007.

[3] P. Corts, G. Ortiz, J. I. Yuz, J. Rodrguez, S. Vazquez, and L. G., "Model Predictive Control of an Inverter With output LC," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1875-1883, 2009.

[4] Poh Chiang Loh, Michael John Newman, Daniel Nahum Zmood, Donald Grahame Holmes, "A Comparative Analysis of Multiloop Voltage Regulation Strategies for Single and Three-Phase UPS Systems," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1176-1185, 2003.

[5] Gustavo Willmann, Daniel Ferreira Coutinho, Luís Fernando Alves Pereira, and Fausto Bastos Líbano, "Multiple-Loop H-Infinity Control Design for Uninterruptible Power Supplies," *IEEE Trans. Ind. Electron.*, vol. 54, no. 3, pp. 1591-1602, 2007.

[6] O. Kukrer, "Deadbeat control of a three-phase inverter with an output," *IEEE Trans. Power Electron.* , vol. 11, no. 1, pp. 16-23, 1996.

[7] M. Kojima, K. Hirabayashi, Y. Kawabata, E. C. Ejiogu, and T. Kawabata, "Novel vector control system using deadbeat-controlled PWM," *IEEE Trans. Ind. Appl.*, vol. 40, no. 1, pp. 162-169, 2004.

[8] P. Mattavelli, "An improved deadbeat control for UPS using disturbance," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 206-212, 2005.

[9] T. Tai and J. Chen, "UPS inverter design using discrete-time sliding-mode," *IEEE Trans. Ind. Electron.*, vol. 49, no. 1, pp. 67-75, 2002.

[10] M. Sun, Y. Wang, and D. Wang, "Variable-structure repetitive control: A discrete-time strategy," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 610-616, 2005.

[11] V. F. Montagner and P. L. D. Peres, "Robust state feedback control applied to an UPS system," in *Proc. 29th Annu. Conf. IEEE Ind. Electron. Soc.*, vol. 3, pp. 2245–2250, 2003.

[12] Q.-C. Zhong, J. Liang, G. Weiss, C. Feng, and T. C. Green, "H_∞ control of the neutral point in four-wire three-phase DC–AC converters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1594-1602, 2006.

[13] "Robust controller design for a single-phase UPS inverter using μ-synthesis," in *Proc. Inst. Electr.Eng. Electr. Power Appl.*, vol. 51, no. 3, pp. 330-340,2004.

[14] José Rodríguez, Jorge Pontt, César A. Silva, Pablo Correa, Pablo Lezana, Patricio Cortés, and Ulrich Ammann, "Predictive Current Control of a Voltage Source Inverter," *IEEE Trans. Ind. Electron*, vol. 54, no. 1, pp. 495-503, 2007.

[15] ZHENG Qing , GAO Zhiqiang, "On Practical Applications of Active Disturbance Rejection Control," in *Proc. 29th Chinese Control Conference*, Beijing,China, pp.6095-6100, 2010.

[16] J. Han, "From PID to Active Disturbance Rejection Control," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 900-906, 2009.

[17] Y. a. W. X. Huang, "Active disturbance rejection control: methodology and theoretical analysis," *ISA Trans.*, vol. 53, no. 4, pp. 963-976, 2014.

[18] Wenchao Xue and Yi Huang, "On Frequency-domain Analysis of ADRC for Uncertain System," in *2013 American Control Conference (ACC)*, Washington, DC, USA, pp.6637-6642, 2013.

[19] G. Herbst, "A simulative study on Active Disturbance Rejection Control (ADRC) as a control tool for practitioners," *Electronics*, vol. 2, no. 3, pp. 246-279, 2013.

[20] Z. Gao, "Scaling and Bandwidth-Parameterization Based Controller Tuning," in *Proc. American Control Conference(ACC)*, Denver, USA, pp.4989-4996, 2003.

[21] A. a. R. I. Yazdani, "Voltage-sourced converters in power systems: modeling, control, and applications", John Wiley & Sons, 2010.

[22] C. e. a. Xing, "Tuning method for second-order active disturbance rejection control," in *Proc. 30th Chinese Control Conference (CCC)* ,Yantai, Chaina , pp.6322-6327,2011.

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