SRPH Journal of Interdisciplinary Studies
Volume 2, Number 3: (6-12), 2020
Available online at: http://sjis.srpub.org/

Analysis the several Techniques in designing the comparators for ADC converter and Introduction the CMOS Comparator Circuit with low power and high speed suitable for Medical Equipments

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Article history:

Received date: 27 May 2020
Review date: 17 July 2020
Accepted date:25 July 2020

Keywords:
Threshold Inverter Quantization, double tail, comparator, slew rate, low power, and kick back noise, dynamic

Abstract
In this paper, several techniques were Analysis in the design of comparators. One CMOS comparator sample is introduced. According to performed simulation, Threshold Inverter Quantization (TIQ) technique is with low manufacturing technology (45 micrometers) and high speed also limitation of adjustment of the suitable reference voltage for the systems within the chip; on the contrary, double tail Technique with low-speed responsiveness and high power in comparation with the other two types, has restriction of use in most of the ADCs. But the introduced circuit despite it has the more formation cost in comparison with the other two techniques but with low power (uW 82) and high speed of performance by taking advantage of kick back noise as well as low slew rate are useable for most of the ADCs used for medical equipments that are portable and need to low power.

Please cite this article as: Jafari E., Jafari M. 2020. Analysis the several Techniques in designing the comparators for ADC converter and Introduction the CMOS Comparator Circuit with low power and high speed suitable for Medical Equipments . SRPH Journal of Interdisciplinary Studies Volume 2, Number 3: (6-12)

Introduction:
Today compares, play an important role in all medical equipments because the need to sampling of vital signs or other body parameters with the appropriate speed is very noticeable. ADC converter is used to convert analog signal to digital in this among that comparators are as a small cell of converters influenced by factors such as offsets of voltage and current in the input and output and kick back noise, slew rate and so on. in these articles [4] [3] [2] [1], several techniques have been investigated in the comparator designing that each one could improve at somewhat the performance with changing several disruptive parameters that are effective in speed and power. Three comparators of TIQ, DOUBLE TAIL and finally a sample of comparator based on preamplifier are introduced that are investigated and compared with simulation their performances.

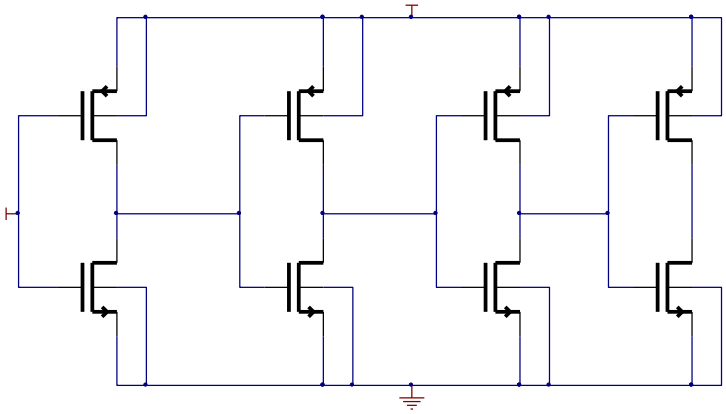


Figure (1) ; IQ Comparator

TIQ Comparator (Figure 1) has been consisted of 4 levels of pair of transistors, that each level is equal the figure (2). In fact, comparison is done in the first two levels, and the next levels (M5, M6, M7, and M8) are responsible for the increasing role of efficacy and increase these levels causes to increase the accuracy and speed. There are no voltage divider resistors in this comparator that resistance error and error of power supply are vanished and reference voltage is determined according to the equation (1) and by changing the length and channel width of transistors that this thing causes to reduce the lack of flexibility in determining the reference voltage.

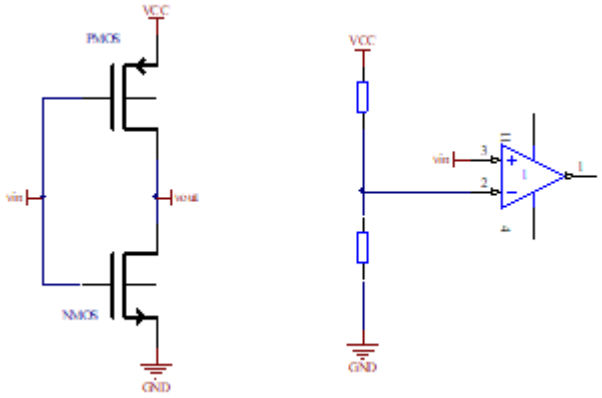


Figure (2)

Reference Voltage is computable from the following equation:

$$V_{Switching} = \frac{\sqrt{\frac{\mu pW_p}{\mu nW_n}}\left[VDD - V_{tp}\right] + V_{tn}}{1 + \sqrt{\frac{\mu pW_p}{\mu nW_n}}} \qquad \text{Equation (1)}$$

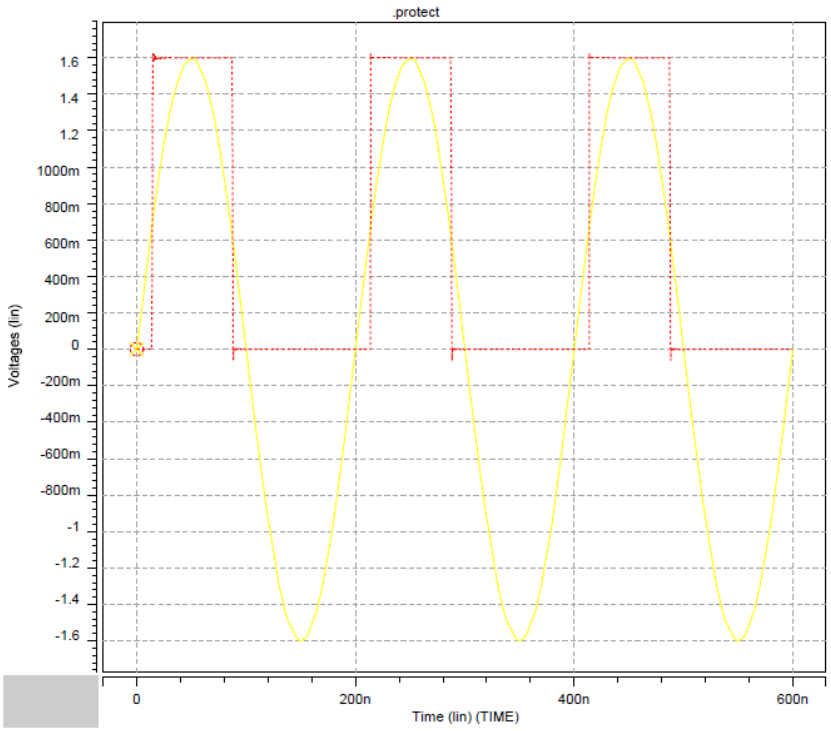
That Wp is the bandwidth of pmos and Wn is bandwidth of the type of vdd and n, is supply voltage, Vtn is the threshold voltage of n-type and Vtp is p-type threshold voltage and it is assumed that the bandwidth of pmos and nmos are equal with each other and whatever the amount of width of channel, the output has faster and more sharp speed, but this may cause the noise ability of output. This technique is more suited for SOC systems. [6] [5].

According to Diagram1, output changes its situation for passing through the mood of the input that the speed of circuit delay can be considered about 1 nanosecond according to the speed of input. It can be concluded of the form of the output wave that there is no need to secondary amplifier level in order to improve the output voltage. The speed and accuracy of comparator can be increased by increasing the number of levels of this comparator that this issue will have direct proportion with the increase in disposability power of comparator. The speed of this comparator sample has reached to 2.2 GHz and disposability power of 145 micro watts without using the clock pulse and the switching.

This comparator such as latch comparator based on pre-amplifier has been composed of a level of preamplifier that is with power switch (Mtail1). The width of this transistor has been considered small to reduce power and reach the low input offset; also width of transistor of Mtail2 that is placed in the output is considered large to reach to quick latch.

Both differential pair transistors are turned off at that time that there is no clock, as a result the transistors of MR and MR2 are turned on by M3 and M4 that makes the output zero, both Tails are turned on at that time that the clock is activated and M4 and M3 and as a result MR1 and MR2 start to turn off and finally differential pair voltage is made in Input .Thereby it will cause to reduce kick back noise and will be created a kind of protection of input.

Diagram (1)



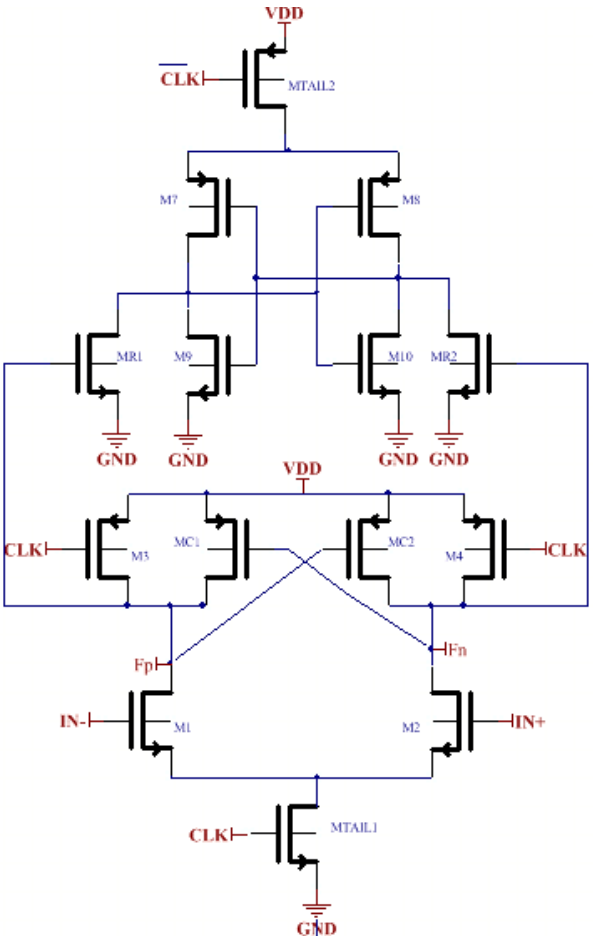


Figure (3); DOUBLE TAIL Comparator

The output is determined in reverse form as 0 and 1 by transistors of M7, M8 M9, and M10. But because of change the amount of nodes of FN, fp from 0 to vdd voltage intermittently, wasting is taking place In terms of disposability power and this waste is eliminated by MC1 and MC2 as a pre charger. [7], [8].

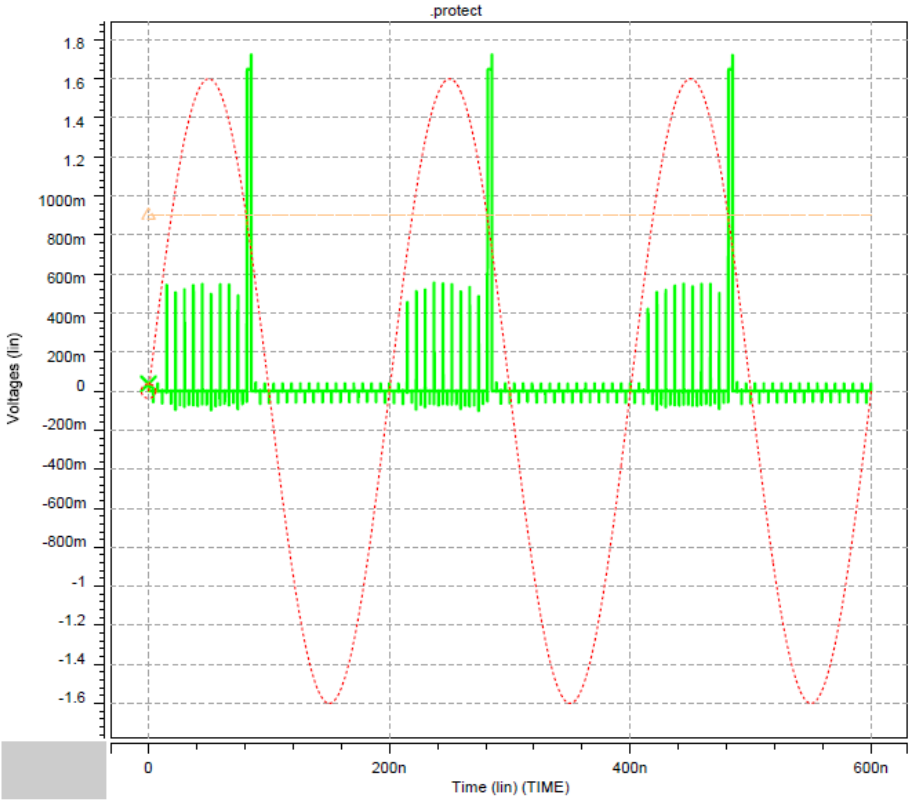


Diagram (2)

Input and output of circuit create one pulse as the amount of vdd according to diagram of simulated circuit at the moment of comparing and at the time that we have ascendant clock for comparing two forms of input waveform of output node. There is need to a double stabilization level that is factor of high disposability power.

The introduction of dynamic CMOS comparator circuit based on the preamplifier

Circuit of Figure (4) is dynamic CMOS comparator based on preamplifier. This circuit has been consisted of a preamplifier with differential inputs and M0 M1 with active loads of M2 M3. Use the pre-amplifier causes to increase the responsiveness speed of output to input actions. The most sensitive part of this circuit that is stabilization includes two back-to-back inverters.

Stabilizer includes transistors of M13 and M5 includes a cross pair of -M7 M6 and performs the action of stabilization, the width rate (240nM) and channel length of CMOS (180 nM) M5 to M8 have been considered minimum to reduce the capacitive property of transistors, and other measures have been optimized based on the middle voltage of feeding. Switching transistor of M11 makes short connection the differential input until the output finds more desire to DC level.

M10 and M9 transistors have been used in order to avoid the compliance of pulses and also kick back noise .width of these transistors also effect on the efficacy of these stabilizers. Increasing the width of these CMOS causes to increase the capacitance property of nodes and its reduction will cause to need to increase the input signal amplitude, In the event of not meeting this need; the balance will not be created in the differential part. The performance of stabilizer consists of two phases of become zero and restoring.

Balance will not be created in becoming zero phase and it is balanced in recovery phase and is strengthening by level of Rail to Rail and recovery cycle is done by NMOS and PMOS, increase in the rate of I bias, causes to increase the output speed of system and this increase in rate will cause to raise the disposability power and

also the frequency responsiveness of the circuit will be very affected by this increase in current. This circuit has been optimized from the perspectives of frequency, power and disposability power.
Wilson reinforced current source has been used in order to have a steady current in positive .

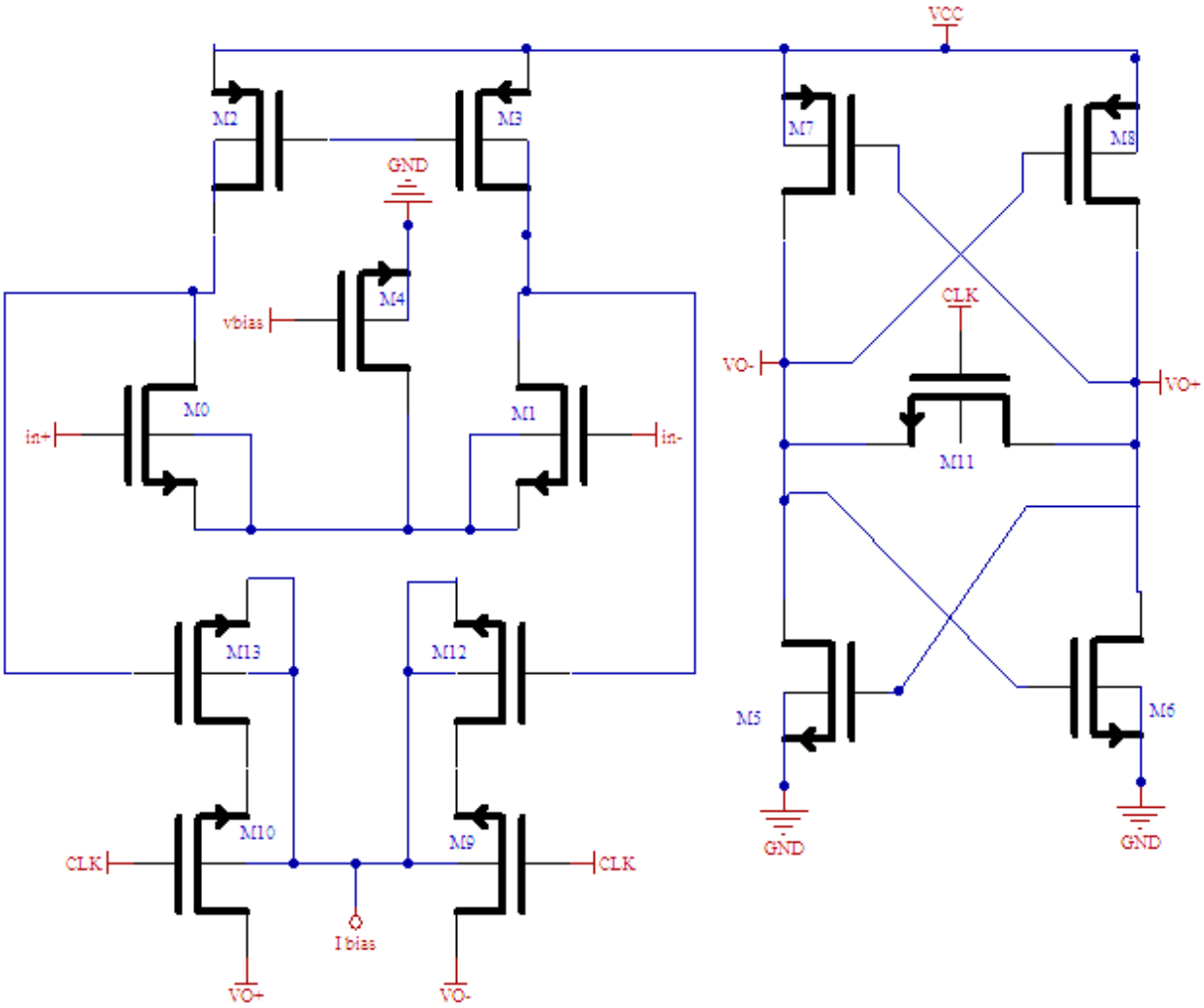


Figure (4)

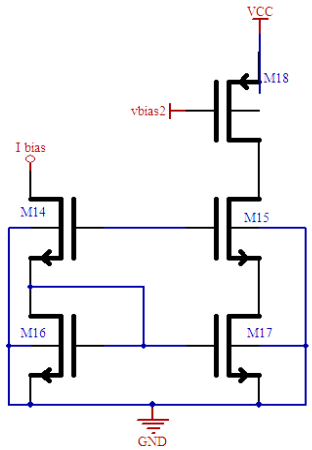


Figure (5) feedback (I bias). Having a steady current causes flat output with sharp edges

Performance of device is visible at high speed and changing in output status for change in Input status and applying the clock pulse in the following diagrams. Fixed reference voltage has been considered 0.9 in these simulations and sinusoidal input comparable voltage has been considered 5MHz with amplitude of 1.6V.

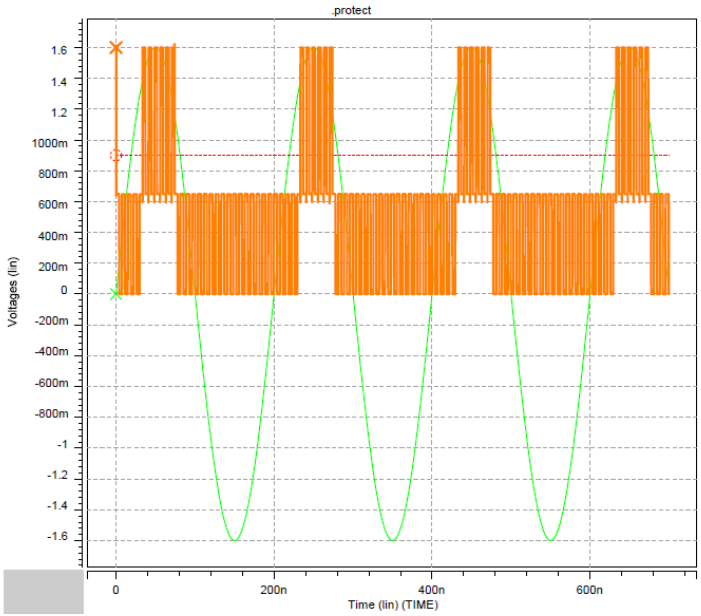


Diagram (3)

As it can be seen in diagram (3) comparator for inputs that positive is larger than negative and the clock pulse allows gives output 1 and gives zero output for the reverse of it. It is quite the opposite for comparator negative output so that this differential output causes that we do not encounter with the problem with the name of time delay dependent to input pulse in the use of flip-flops in the output part of circuit and we have high-speed stabilized output comparator. According to performed simulation the Wilson current source shows the best performance with produce the current of 1n amps and bias voltage of 1.4 volts and also at the maximum frequency of launch of 135.1 MHz in power of 82.4uW. In diagram 4 the above curve shows total disposability rate of comparator in 1.6V voltage.

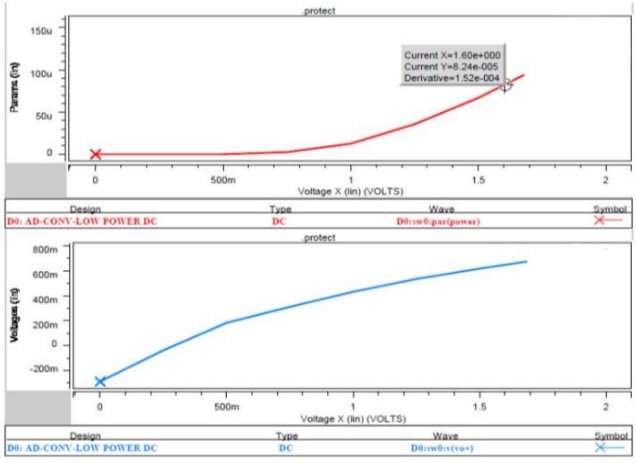


Diagram (4)

Table (1)

Price	The use in circuits of ADC	flexibility	Working frequency	Disposability power	Slew rate	offset	Kick back noise	Bias current Input and out put	Type
Cheap	system SOC	X	Unlimited	145 uw	Quick	Very low	Has	X	TIQ
Average	Most of the systems	Low	100MHz	126uw	Slow	Has	Has	Low	DOUBLE TAIL
Expensive	Most of the systems	High	135.1Mz	82.4uw	Average	Low	Very low	Low	Suggested

Conclusion

The speed was increased addition to reducing the power in TIQ technique but its biggest limitation is making stable and fixed the reference voltage during the design that it causes that this technique is used more in systems within the chip. These types of comparators have nearly more wastes of power in terms of disposability power because they are always on and there is no control in turning on and off the sampling but they are significant in terms of speed compared to other comparators. Double Tail that was particular way that was forced the differential pair comparison of a pair of inverters to compare for better output. In the observed simulation that the output is in pulse form that needs to strengthen and stabilize, another case is this that compared to other methods that had further delay in responsiveness or recognition also kick back noise is reduced in proposed comparator despite the existence of preamplifier and the speed of responsiveness has been also high that is suitable for battery-operated sampling equipments, particularly medical equipments. The parameters affecting the performance of several comparator techniques with proposed circuit have been shown in following table.

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