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"Research Note"

A NOVEL APPROACH TO THE PLATINUM ELECTRODE ETCHING FOR DRAM APPLICATIONS*

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Abstract – We have proposed the novel etching technology of Pt using a hard mask in reactive ion etching plasmas. By the insertion of a Ti mask layer and increasing the wafer temperature in O_2 plasma by a dual frequency reactive ion etcher (RIE), we have obtained a higher Pt etching slope. This result not only enlightens the next generation of DRAM and FRAM technology, but also develops the basic technology of patterning inert materials.

Keywords – Ti mask, etching, scanning electron microscopy, transmission electron microscopy

1. INTRODUCTION

In recent years, in order to increase a storage capacity per cell for 4 Giga-bit dynamic random access memory (DRAM) and beyond, the usage of a barium strontium titanate (BST) capacitor has been considered [1, 2]. In the fabrication of a ferroelectric random access memory (FRAM) device which has attracted great attention for non-destructive read-out type non-volatile memory applications, the lead zirconium titanate (PZT) or $SrBi_2Ta_2O_9$ (SBT) capacitor has been studied [3, 4].

As an electrode material for BST, PZT, and SBT capacitors, various materials such as platinum (Pt), iridium (Ir), ruthenium (Ru), ruthenium oxide (RuO_2) and iridium oxide (IrO_2) have been investigated. Among them, Pt is one of the most appropriate materials because of its good oxidation-resistance, high electrical conductivity, and low leakage current [5].

In order to use the Pt as an electrode material in the stacked capacitor cell structure successfully, Pt etching has been studied [6, 7]. For device application, the separation (shown in Fig. 1) between two adjacent bottom electrodes should be wide enough, because the following steps of the BST and the top electrode Pt deposition need to be accomplished and because the electrical short should be avoided. At the same time, the top area of the Pt electrode should not be reduced significantly in order to ensure a sufficient capacitance area and thus satisfy the required storage capacity per cell. In order to obtain the sufficient bottom separation and the capacitance area simultaneously, a high enough etching slope of Pt electrode is required.

However, as Pt has a low reactivity and its etching products have low vapor pressures, the etching of Pt proceeds by physical sputtering, resulting in a low etching slope [8]. Accordingly, as the adjacent electrodes are connected with Pt, the bottom Pt electrodes cannot be separated from their adjacent electrodes, especially in a small critical dimension (CD) pattern (Fig. 2).

In this study, we have used O_2 plasmas in a reactive ion etcher (RIE) for fabricating the Pt bottom electrode of 0.40 μm CD pattern for DRAM device. We increase the wafer temperature by employing the dual frequency RIE method. The combination of high RF power (13.56 MHz) and low RF power (450 kHz)

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results in high-energy ion bombardment, and thus raises the wafer temperature. We investigate the effect of titanium (Ti) mask layer insertion between the Pt and SiO_2 hard mask, and also investigate the effect of wafer surface temperature on the etching slope of the Pt electrode.

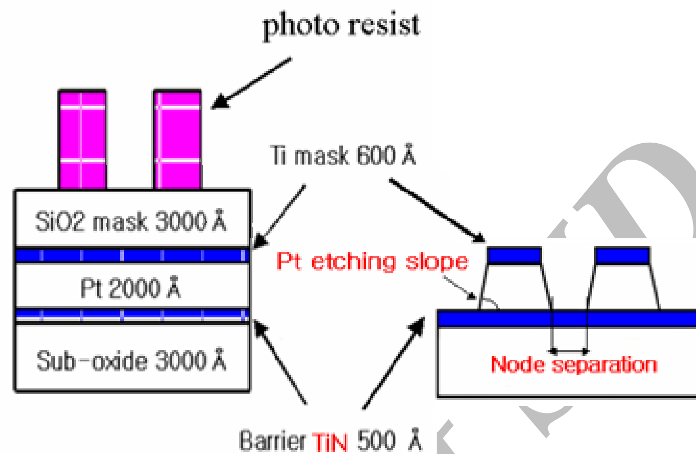

Fig. 1. The sample structure with substrate/TiN (600 Å)/Pt (2000 Å)/mask Ti(600 Å)/mask SiO_2 (3000 Å) a) before opening the mask. b) after the Pt etching

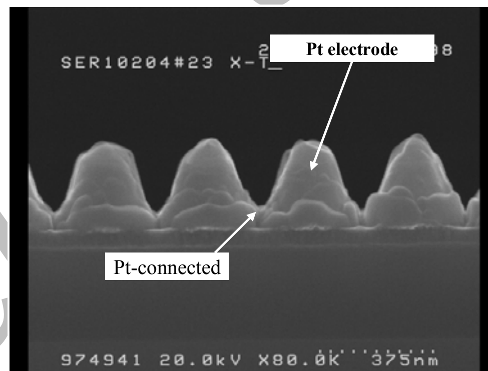

Fig. 2. Cross-sectional SEM images of Pt electrode structures patterned with conventional (SiO_2) mask without Ti layer. Low etching slopes with sidewall residues are observed with the bottom Pt electrodes connected

2. EXPERIMENTAL

The sample structures before and after opening the hard masks are shown in Fig. 1. After patterning the SiO_2, mask using $CF_4/CHF_3/Ar$ gas, which is the first mask for the Pt etch, the photoresist was removed. The Ti layer, as a second mask for the underlying Pt, was patterned by the Ar/Cl_2 gases using the SiO_2 mask. In our Pt etching process, the Pt etch process consists of a main etch step stopped at end point detection (EPD) and an 100%-over etch step to remove the Pt residues. Then the barrier TiN layer was removed by etching with Ar and Cl_2 gases.

3. RESULTS AND DISCUSSION

In order to investigate the effect of wafer temperature on the Pt etching using O_2 plasma, we have performed the patterning experiments at 80°C and at 220°C. Figures 3a and 3b show the cross-section of Pt electrode structures patterned at 80°C and at 220°C, respectively, with 100% overetch after EPD. The SEM images indicate that the Pt etching slopes are about 70°C and 80°C, respectively, at the substrate temperature of 80°C and 220°C. The TEM image reveals that the volume of the remaining Ti mask layer is larger at an

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etching temperature of 220°C than at 80°C. We thus surmise that the lesser erosion of the Ti mask layer during etching plays a crucial role in obtaining the high Pt etching slope. Furthermore, closer examination of the TEM image reveals that the Ti mask can be divided into the outer whitened region and the inner blackened region. The energy dispersive spectroscopy (EDX) spectrum indicates that the whitened region has a considerable amount of oxygen besides titanium, while the blackened region contains little oxygen and is composed mostly of titanium (not shown here). The Ti mask etched at 220°C has a larger volume of whitened region compared to that etched at 80°C. What has to be noticed is that the whitened region, which contains a considerable amount of oxygen, increases by increasing the etching temperature.

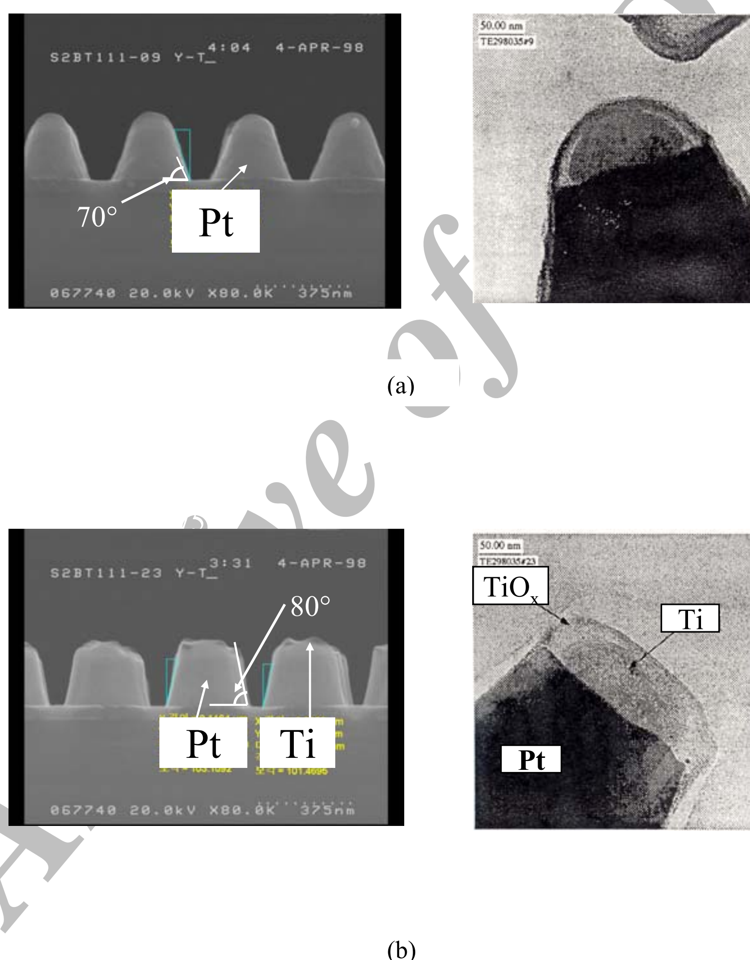

Fig. 3. Cross-sectional images of Pt electrode structures patterned using O_2/Cl_2 plasmas with the TiN mask layer a) At the substrate temperature of 80°C. b) At the substrate temperature of 220°C. All samples were 100%-overetched after EPD.
Left: SEM images. Right: TEM images

In order to investigate the changes induced in the Ti layer during the Pt etching process, we have employed the O_2 plasma treatment on the Ti surface of the blanket wafer at 220°C. The treatment time and conditions were exactly the same as the actual etching process. The XPS data of the Ti surface below the depth of about 100 Å both before and after the Pt etching process at 220°C, reveal that most of Ti-Ti bonding has disappeared and probably changed to the Ti-O bondings after the Pt etching process, indicating that the Ti layer has been transformed to the TiOx layer at least up to 100 Å.

We surmise that the Ti mask layer is exposed after the erosion of the SiO_2 mask. Since the edge Section of the Ti mask is exposed earlier in oxygen plasma due to the earlier disappearance of the SiO_2 mask, more oxygen is diffused into the edge section of the Ti mask. The efficiency of oxygen diffusion is higher at the

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higher temperature etching and the Ti mask etched at 220°C has a larger volume of the region, which is considered as TiOx, than that etched at 80°C.

It is beyond our knowledge why the oxygen diffusion and the change of the Ti layer to the TiOx layer are related to the lesser erosion of the Ti mask. We estimate that for the Ti-O reaction occurring during the etching process, the oxygen species from the plasma is consumed and thus less oxygen is used for the sputtering of the Ti mask. In this case, the Pt etching slope can be increased continuously by sputtering off the Pt atoms with the hard mask remaining. More systematic study is necessary to reveal the detailed mechanism.

4. CONCLUSIONS

To summarize, we have demonstrated that the combination of the Ti mask layer with the oxygen in the plasma at elevated temperatures raised by employing the RIE can contribute to the efficient etching of inert materials such as Pt. At higher etching temperatures, a lesser amount of the Ti mask layer is eroded during etching and this contributes to obtaining the higher Pt etching slope.

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REFERENCES

1. Hwang, C. C., Juang, M. H., Lai, M. J., Jaing, C. C., Chen, J. S., Huang, S. & Cheng, H. C. (2001). Effect of rapid-thermal-annealed TiN barrier layer on the Pt/BST/Pt capacitors prepared by RF magnetron co-sputter technique at low temperature. *Solid State Electronics, 45*, 121.
2. Hwang, C. S. (1998). (Ba, Sr)TiO_3 thin films for ultra large scale dynamic random access memory. A review on the process integration. *Mater. Sci. Eng. B, 56*, 178.
3. Minamikawa, T., Yonezawa, Y., Heya, A., Fujimori, Y., Nakamura, T., Masuda, A. & Matsumura, H. (2001). Preparation of SiN_x passivation films for PZT ferroelectric capacitors at low substrate temperatures by catalytic CVD. *Thin Solid Films 395*, 284.
4. Zhu, X., Liu, Y., An, Z., Zhu, T., Wu, T. Z., Yu, T., Liu, Z. & Ming, N. (2000). Characteristics of $SrBi_2Ta_2O_9$ thin films prepared by pulsed laser deposition for non-volatile memory applications. *Thin Solid Films 375*, 200.
5. Saito, S. & Kuramasu, K. (1992). Plasma etching of RuO_2 thin films. *Jpn. J. Appl. Phys. 31*, 135.
6. Baborowski, J., Muralt, P., Ledermann, N. & Hiboux, S. (2000). Etching of RuO_2 and Pt thin films with ECR/RF reactor. *Vacuum 56*, 51.
7. Wuu, D. S., Kuo, N. H., Liao, F. C., Horng, R. H., Lee, M. K. (2001). Etching of platinum thin films in an inductively coupled plasma. *Appl. Surf. Sci*., *638*, 169-170.
8. Yoo, W. J., Hahm, J. H., Kim, H. W., Jung, C. O., Koh, Y. B., and Lee, M. Y. (1996). Control of etch slope during etching of Pt in Ar/Cl_2/O_2 plasmas. *Jpn. J. Appl. Phys. 35*, 2501.

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