

A HIGH SPEED SiGe VCO BASED ON SELF INJECTION LOCKING SCHEME*

N. SANIEI^{1**} AND H. DJAHANSHAHI²

¹ Faculty of Electrical and Computer Engineering, Shahid Beheshti University (SBU)
Evin, Tehran, I. R. of Iran, 1983963113

Email: namdar@ieee.org

² PMC-Sierra, 100 – 2700 Production Way, Burnaby BC, V5A 4X1, Canada

Abstract– This paper discusses the design and implementation of an inductorless differential VCO with a maximum oscillation frequency of 20 GHz, in a 47 GHz SiGe process technology. The VCO is based on a full-wave rectification frequency-doubling technique, applied to a half rate differential single-stage feedback oscillator. It also benefits from a new circuit phenomenon named hereinafter Self Injection Locking (SIL). The implemented VCO has an area of 0.5 mm² and features a remarkably high ratio of VCO frequency to process f_T . Based on measurement results, the VCO consumes a DC power of less than 165 mW and exhibits a phase noise of -96 dBc/Hz at 1 MHz offset.

Keywords– Silicon germanium (SiGe), heterojunction bipolar transistor (HBT), high-speed circuit, voltage-controlled oscillator (VCO), phase noise, differential stage, injection locking oscillator

1. INTRODUCTION

Voltage controlled oscillators (VCOs) are widely used in many multigigahertz or multigigabit per second systems such as clock-and-data recovery and clock synthesizer PLLs. SiGe technology is a good candidate for implementing very high frequency circuits compared to CMOS technology. This is due to the fact that for the same unity current gain cut-off frequency, f_T , SiGe transistors have larger feature sizes. As a result, the cost of fabrication, which is highly affected by the size and number of lithography masks, will be reduced.

While most high frequency VCOs, reported in the literature use some form of LC tank or resonator to achieve good phase noise performance [1, 2] they often occupy a large die area and have a very limited tuning range. The VCO presented in this work is an inductorless ring-type oscillator implemented in a 47 GHz SiGe Heterojunction Bipolar Transistor (HBT) technology and features up to 20 GHz output frequency, a relatively small area, a good tuning range, and a phase noise performance comparable to most reported resonator-type VCOs [1, 2].

The VCO is designed and implemented based on doubling the frequency of a half-rate VCO, which is implemented by itself as a standalone VCO test chip. The 20 GHz VCO, in addition to the doubling technique, benefits from a special kind of injection locking mechanism, as briefly described below.

Injection locking is a well-known and long-studied subject for oscillators [3, 4]. In these oscillators an external source injects a signal with a frequency higher, lower or equal to the oscillator free-running frequency (Fig. 1a). If the oscillator has proper characteristics, it will lock onto the injected signal changing the free running frequency of the oscillator, accordingly. A similar phenomenon, however, with

*Received by the editors November 4, 2006; final revised form October 22, 2007.

**Corresponding author

an internally generated doubled frequency signal (Fig. 1b) is observed in the VCO discussed in this work that is named hereinafter *Self Injection Locking (SIL)*. This circuit phenomenon is being reported for the first time.

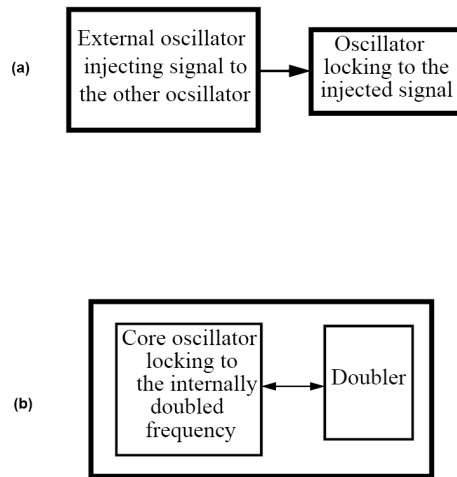


Fig. 1. a) An oscillator locking on to the externally injected signal from another oscillator, b) an oscillator locking on to the internally injected signal from the doubler

In section 2 of this paper the theory and design details of the proposed VCO are described. Section 3 presents the experimental results, and is followed by a conclusion in section 4.

2. VCO DESIGN

The VCO core used in this work, as shown in the dashed circle of Fig. 2, is similar to the core oscillator previously proposed by the authors and implemented in InP HBT technology [5]. In the core oscillator, a cascode amplifier is followed by an emitter follower in a closed loop, thus producing a feedback oscillator also known as a single-stage ring oscillator. The ring oscillator (RO) terminology comes from the fact that one can implement multi-stage RO using N stages of the same delay cell, where the delay cell is the open-loop version of the core oscillator in Fig. 2. Bias currents are supplied by the current mirrors at the tail of each branch to set the operating points near the peak, f_T , of the transistors. A change in the bias currents varies the oscillation frequency. To maintain the oscillation, Barkhausen's criteria must be met. Fig. 3 illustrates the gain/phase (ac) response of the open-loop core oscillator. It shows that the core oscillator attains an additional phase shift of 180 degrees at a frequency near 15 GHz. This corresponds to a small signal gain of about 10 dB as shown in Fig. 3. While Fig. 3 reflects the results of small signal analysis of the core oscillator, large signal (transient) simulations reveal that the core can oscillate with a maximum frequency of about 14 GHz.

• 20 GHz VCO with differential outputs

In the first step of the design, a 13 GHz differential VCO was developed from the core oscillator as shown in Fig. 2. A voltage-to-current converter was added to the core oscillator to control the current mirrors providing bias for different branches of the circuit. The resistors used in the current mirrors are chosen to optimize signal power and noise, while increasing the impedance of the tail current sources. To isolate the core oscillator from the loads an output buffer is used as shown in Fig. 2. The buffer loads the core oscillator, reducing the maximum oscillation frequency from 14 GHz to about 13 GHz. The output buffer is a differential pair with a gain designed to maximize signal swing at the output. The outputs of the

differential pair buffer are terminated by $50\ \Omega$ resistors on chip to better match the input resistance of measurement equipment [6, 7]. This leaves the emitter degeneration resistor, connecting the emitters of the output buffer transistors, as the main design parameter to control the gain of the buffer. The degeneration resistor affects the gain, noise and linearity of this stage.

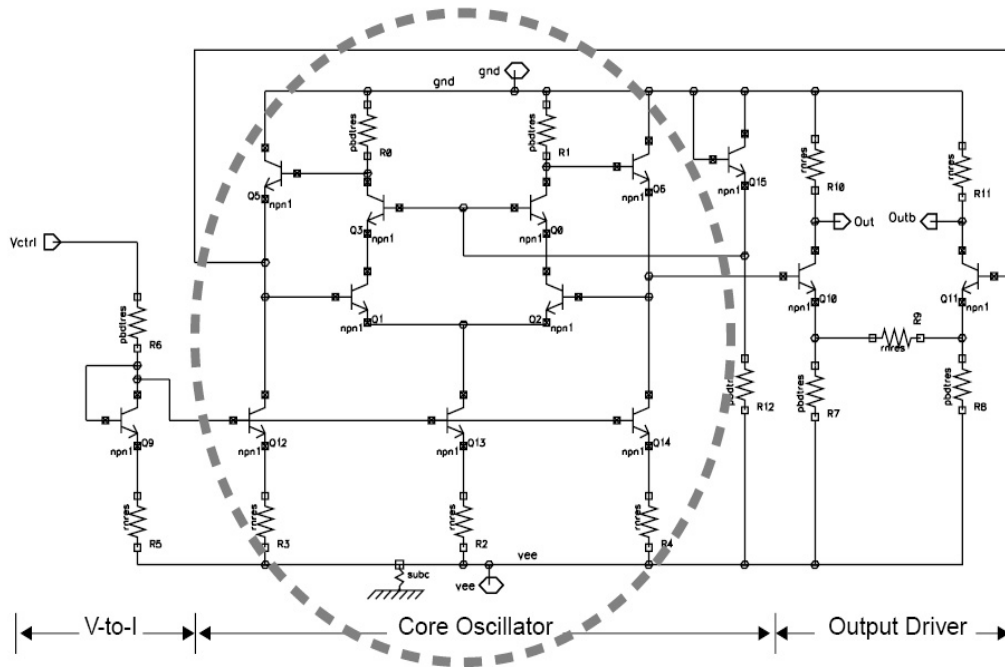


Fig. 2. Fundamental-rate (13 GHz) differential VCO

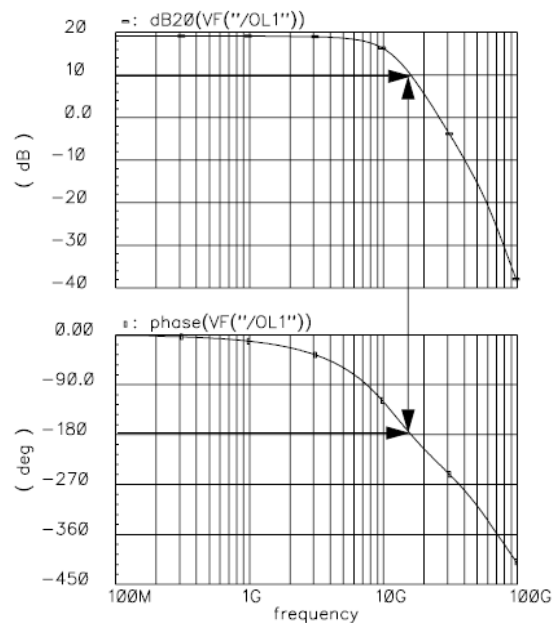


Fig. 3. Gain/phase (ac) response of the open loop core

As the second step of the design, a 25 GHz VCO [8] was designed and implemented by simply converting the output buffer of the 13 GHz oscillator to a two-diode full-wave rectifier, as shown in Fig. 4. In this circuit though, as reported in [8], a weak first harmonic (12.5 GHz) was still present, the tuning range was small and the output power was largely frequency dependent. Moreover, the output was single ended, which is often not satisfactory for a noise immune circuit design. As a consequence, in the next step of the design a VCO with differential outputs was designed as explained in the following.

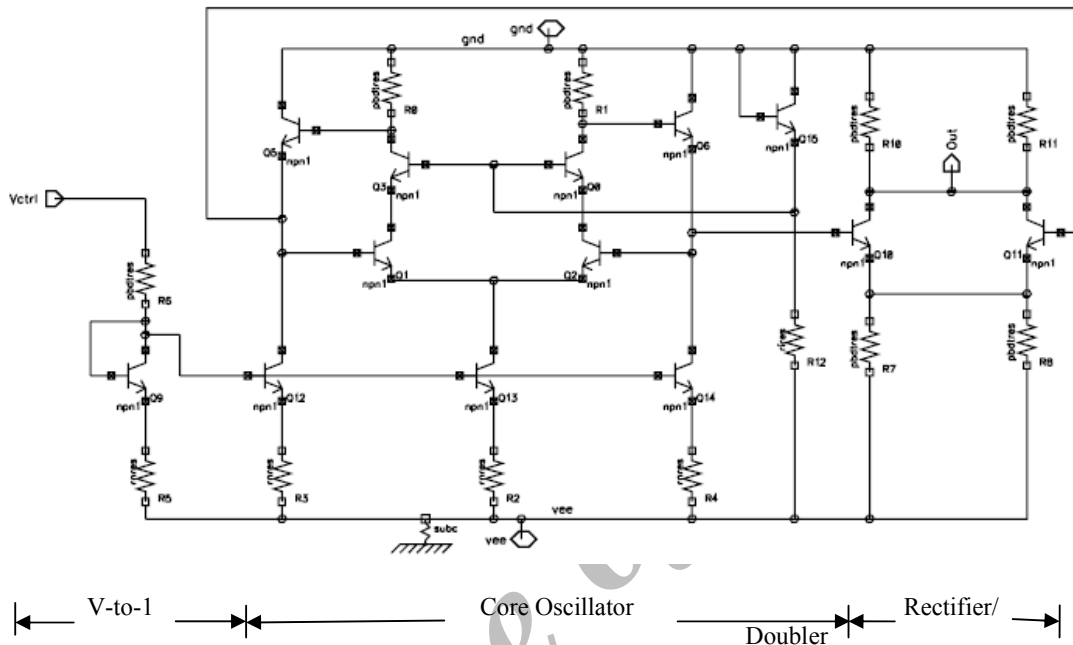


Fig. 4. Schematic of the 25 GHz VCO (the first design [8] based on two-diode rectifier/doubler)

The two-diode rectifier frequency doubling technique can be extended to use a four-diode (diode bridge) full-wave rectifier. Fig. 5 illustrates the schematic of such VCO. This circuit is comprised of 19 npn HBT SiGe transistors and 12 polysilicon resistors where resistors are implemented over a deep-trench maze to reduce parasitics [9]. The HBTs have single and double emitter strips, with areas ranging from 5 to 10 squared microns. The voltage to current converter and the core oscillator are, in most parts, similar to the previous VCO. The only difference is the addition of 50 Ω resistors on the collectors of the emitter-followers in the core oscillator in order to drive the output loads. Therefore, the output loads may be driven by the core directly. However, the buffer stage is modified such that it rectifies the two differential signals from the core oscillator and produces two complementary outputs at double the frequency. While operating as a full-wave rectifier the output of the core oscillator (Out1, Out1b) is also buffered, making it possible to drive the next stage (e.g. feedback path in a PLL) and monitor the clock simultaneously. The buffered outputs of the doubler are denoted by Out2 and Out2b, as shown in Fig. 5.

In Fig. 5 the diodes shown in dashed circles form the diode bridge, while the other four diode-connected transistors in a ladder type architecture provide symmetrical bias voltages for the doubling circuitry. The VCO operates at a maximum frequency of 20.5 GHz. The maximum frequency of the half-rate VCO is somewhat smaller than the original (13 GHz) value due to the additional loading effect of the doubler circuitry. The maximum oscillation frequency of the core oscillator reduces to about 10 GHz when loaded by the diode bridge full-wave rectifier doubler. This is mainly due to additional parasitic capacitances of the doubler, as well as the smaller input impedance of the doubler stage.

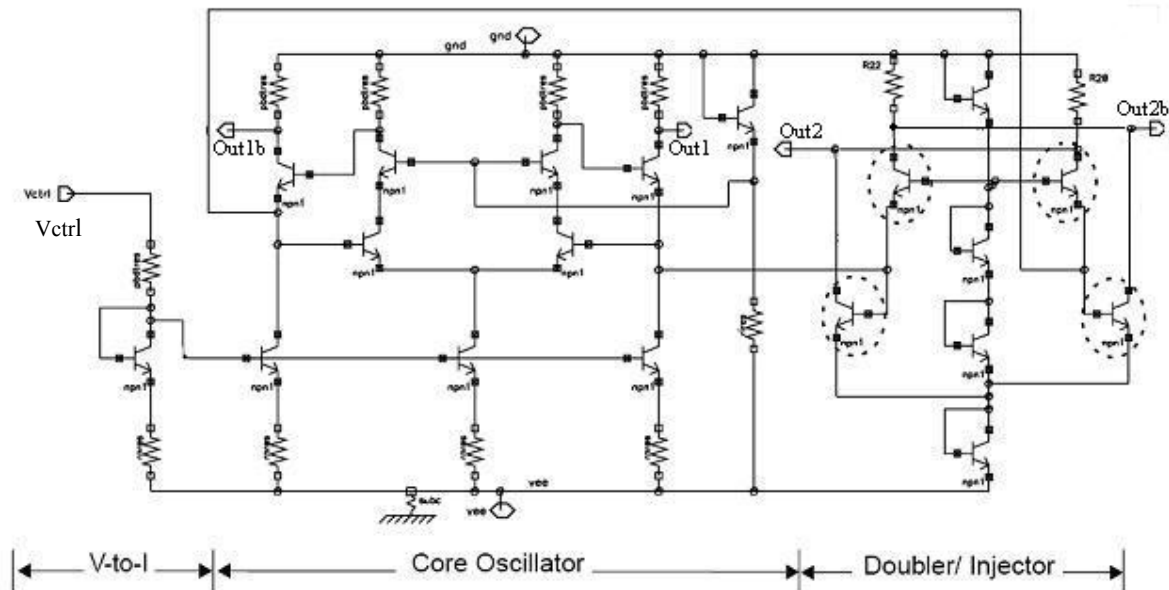


Fig. 5. Schematic of the 20 GHz VCO (improved design based on four-diode doubler)

Using the translinear circuits principle (TLP) [10], it can be shown that the outputs of the diode bridge doubler are complementary or 180 degrees out of phase. Having differential outputs is one major advantage of this VCO, in contrast with the single-ended output in the 25 GHz VCO of Fig. 4 [8].

In principle, the operation of this VCO (Fig. 5) is rather interesting and different from the 25 GHz VCO. In this circuit the core oscillator also oscillates at a maximum rate of 20.5 GHz, due to a Self Injection Locking (SIL) phenomenon observed in the circuit. Precisely speaking, the core initiates oscillations with a frequency around 10 GHz, but as soon as the signal is doubled by the full-wave rectifier and fed back (injected) to the core, it locks on to the doubled frequency signal and oscillates with a frequency of about 20 GHz. At this point the 20 GHz signal generated by the core is doubled through the diode bridge to a frequency near 40 GHz; however, since 40 GHz is relatively close to the unity gain frequency of the process technology it is highly attenuated by the low-pass nature of the devices and cannot cause the core oscillator to lock on to it. On the other hand, the two top transistors as well as the two bottom ones in the diode bridge form two differential pair amplifiers and both amplify the 20 GHz signal produced by the core oscillator. Needless to say, the core oscillator and the doubler (diode bridge rectifier) must meet certain conditions for this circuit to operate, as explained next.

In order to maintain a wide locking range to an externally injected signal, an oscillator has to meet the following requirements [3]:

1) The oscillator must have a very low quality factor, Q .

The low Q disadvantage of ring oscillators is turned around as a benefit in this circuit. Based on the slope of the phase response w.r.t. frequency ($d\phi/d\omega$), the Q of this VCO is estimated to be close to one [11], which is considered a very low Q .

2) Phase difference between the oscillator and injected signal, α , must fall in the range of $\pm\pi/2$. The phase difference, α , is described by the following equation [3]:

$$\sin(\alpha) = 2QE \Delta f_o / (E_{inj} \cdot f_o)$$

where E_{inj} is the injected signal amplitude, E the oscillator amplitude, f_o is the free running frequency of the core oscillator and Δf_o is the difference between the oscillator free running frequency and the injected frequency. For this doubler circuit, Δf_o is equal to the free running frequency, f_o . Thus to meet the phase requirement the following condition must hold:

$$|E_{inj}/E| > 2Q$$

Simulations indicate that the output of the doubler which is fed back to the core oscillator has nearly 3 times the amplitude of the oscillator output [11]. This results in a sufficiently large amplitude ratio, E_{inj}/E , to satisfy the condition mentioned above, given the low- Q oscillator with $Q \approx 1$.

Thus the doubling mechanism of diode-bridge rectification in conjunction with the low Q single-stage core oscillator used in the VCO of Fig. 5, provide the necessities for the oscillator to lock on to the signal generated by its doubling circuitry. The authors call this new circuit phenomenon a Self Injection Locking (SIL) of the oscillator to its second harmonic.

3. EXPERIMENTAL RESULTS

Both the half-rate VCO and the doubled 20 GHz VCO are fully differential and are implemented with a symmetrical layout to reduce the effect of common mode noise, substrate and supply noise. In addition to noise, symmetry also helps suppress the fundamental and odd frequency harmonics, thus reducing the total harmonic distortion (THD) in the circuit. A ground plane is formed by the first metal layer to isolate the substrate from other layers as much as possible (metal shield). Two metal-insulator-metal (MIM) capacitors are also used to by-pass the DC bias of the core cascode transistors. The interconnect lengths have been kept as short as possible (less than $\lambda/8$) to avoid transmission line effects. In fact, the longest interconnect used here is near 150 microns, less than a quarter of what would be considered a transmission line in such a circuit [7].

The circuits were tested on a wafer using 40 GHz probes and a 50 GHz spectrum analyzer. The spectrum of the half-rate VCO near 13 GHz frequency is shown in Fig. 6a. Also as indicated on the figure, the phase noise of the VCO at 1 MHz offset is about -90 dBc/Hz. This was also verified by the phase noise measurement utility of the spectrum analyzer. The measured results indicate that the frequency can be swept from about 8 GHz to above 13 GHz, as shown in Fig. 6b. The average gain of the VCO, with respect to control voltage input ($K_{vco} = \Delta f / \Delta V_{ctrl}$), is approximately 3 GHz/V. Signal power was measured at one output while terminating the other output by a 50 Ω load. The power delivered into a 50 Ω load at each output varies from -34 dBm up to about -4 dBm. The measured output frequency and power plots are overlaid in Fig. 6b.

The 20 GHz VCO is implemented in a pad-frame with the same dimensions as the half-rate VCO and hence occupies the same die area; i.e. $810 \mu\text{m} \times 620 \mu\text{m}$ ($= 0.50 \text{ mm}^2$ including the pads). While the active area of the half-rate VCO is $150 \times 150 \mu\text{m}^2$, the active area (excluding the pads) of the 20 GHz VCO is larger by an amount of $90 \times 70 \mu\text{m}^2$ due to the area occupied by the doubler. The micrograph of the 20 GHz VCO is shown in Fig. 7. In this VCO the outputs are taken from the collector of emitter followers in the core oscillator; thus avoiding an additional buffer at the outputs of the doubler. A version of this circuit with an output buffer for the doubler was also implemented. Measurement results of this circuit are quite similar to those from the circuit without a buffer. Therefore, in this paper the results are reported only for the VCO without the additional buffer, which is more power and area efficient.

The full spectrum of the VCO depicted in Fig. 8 shows no half-rate component (near 10 GHz) due to the locking of the core oscillator to the frequency of the doubler. The VCO output spectrum near 20 GHz is also shown in Fig. 8. The only harmonic visible in the spectrum is the $4f$ component, 39 GHz, with a

power reduced to about -35 dBm, which is 25 dB below the desired $2f$ component. Elimination of the fundamental harmonic f is one of the most important features of this VCO.

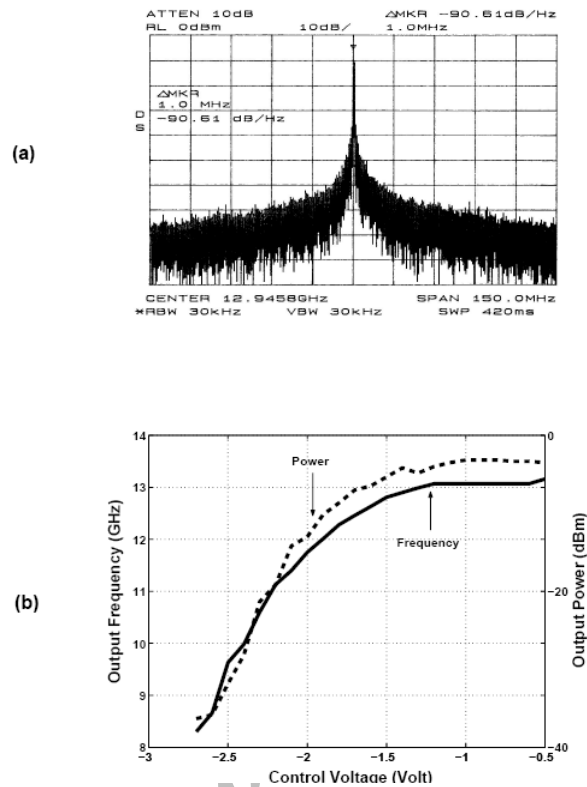


Fig. 6. a) Spectrum of the fundamental-rate VCO, near 13 GHz, b) measured output frequency and power at each output

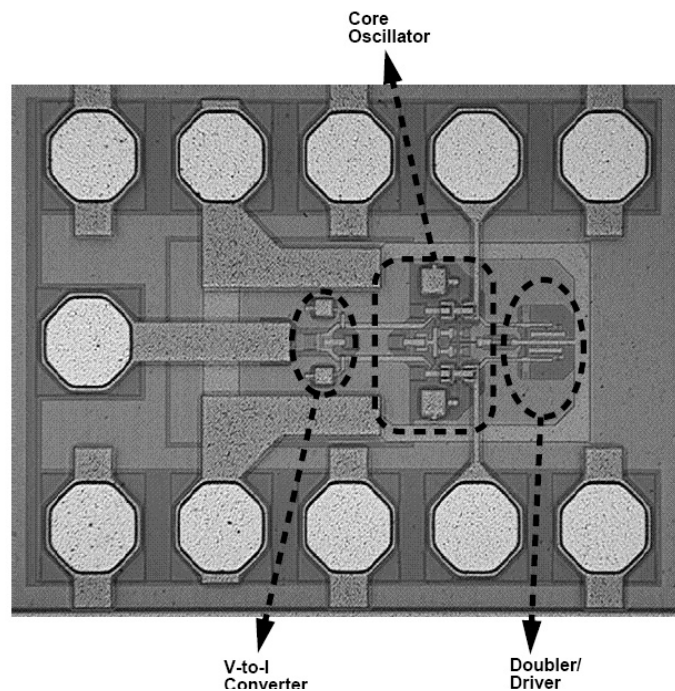


Fig. 7. Micrograph of the 20 GHz VCO

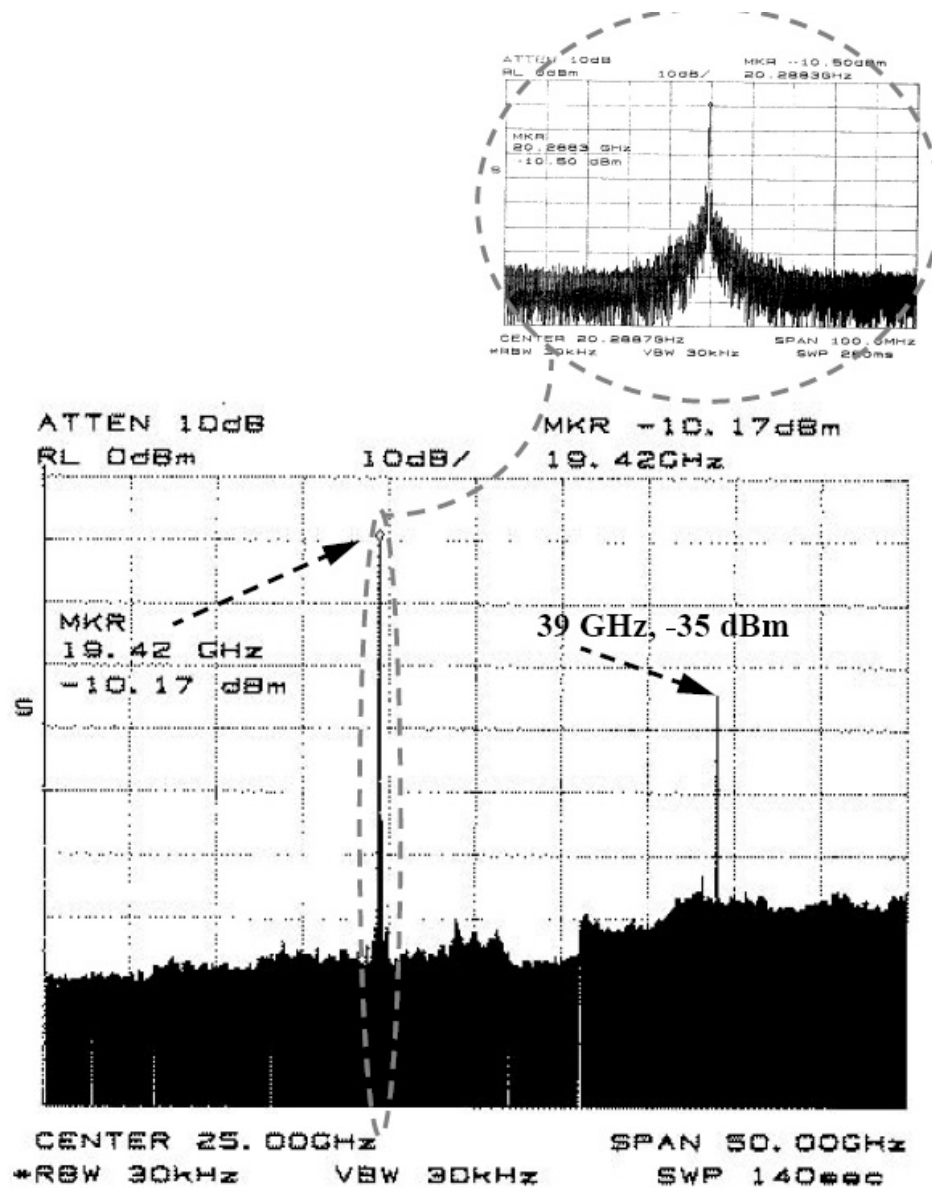


Fig. 8. Full spectrum of the 20 GHz VCO, and the spectrum near 20 GHz

Measurement results show a relatively wide frequency tuning range, from 12 to 20 GHz, for 1.7 Volts change in the control voltage (Fig. 9a). The average VCO gain w.r.t. control voltage is about 4.7 GHz/V. Increasing the absolute supply voltage to 3.5 Volts can easily push the maximum output frequency above 21 GHz. The output power is also graphed in Fig. 9a. While the output power varies from -22 dBm to about -10 dBm, it is relatively constant between -10 to -15 dBm for a major portion of control voltage adjustment. In addition to providing differential outputs, exhibiting a wide tuning range and eliminating the half-rate (main harmonic) frequency component, a fairly constant output power is another advantage of the 20 GHz SIL-based VCO over the single ended 25 GHz VCO reported in [8]. The DC power dissipated by this circuit is approximately 165 mW. The phase noise of this VCO vs. offset frequency is shown in Fig. 9b. At 1 MHz offset the phase noise is better than -96 dBc/Hz. Improvement in phase noise is due to the nature of injection locking oscillators that can be modeled as a first order PLL [12], thus attenuating a portion of the phase noise in the VCO.

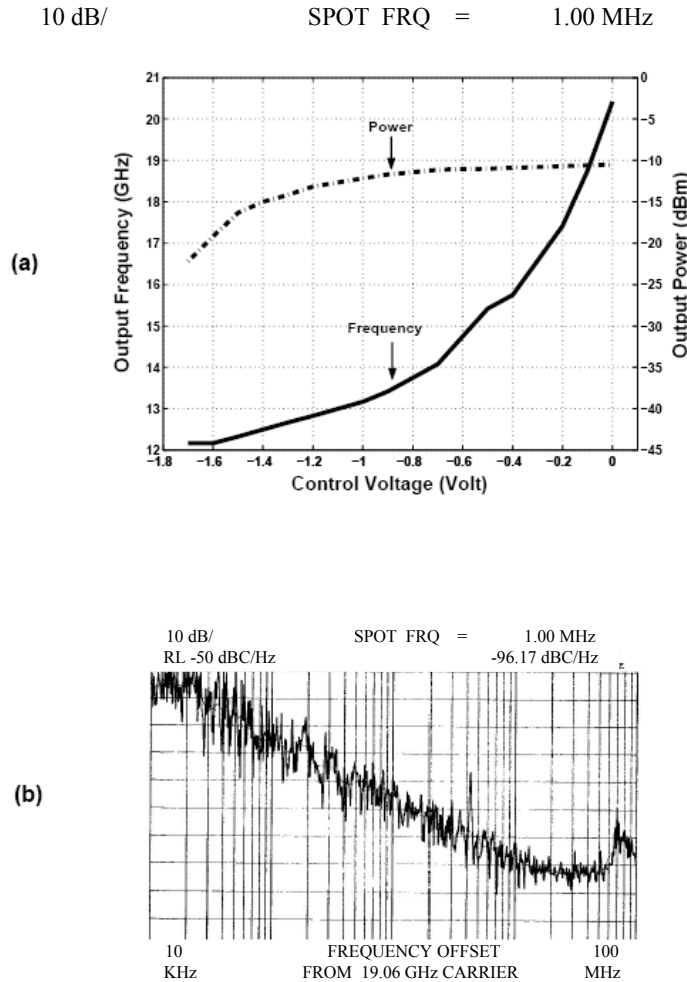


Fig. 9. a) Measured output frequency and power of the 20 GHz VCO, b) measured phase noise of the 20 GHz VCO vs. offset frequency

4. CONCLUSION

Design and implementation of an inductorless VCO with a maximum oscillation frequency of 20.5 GHz in a 47 GHz SiGe HBT technology was demonstrated. A full-wave rectification scheme was used to double the core frequency of a half-rate VCO and achieve the 20 GHz frequency with a tuning range of 8 GHz. In addition to the diode bridge doubling technique an interesting new circuit phenomenon named *Self Injection Locking (SIL)* was also responsible for the operation of the implemented VCO. The VCO based on the diode-bridge frequency doubling technique exhibited a wide tuning range, with fairly constant output power, while eliminating the fundamental harmonic and providing differential outputs. The layout of the VCO was symmetrical to improve phase noise performance and reduce harmonics. The circuit layout was pad limited and the VCO circuitry occupied an area of $810 \mu\text{m} \times 620 \mu\text{m}$, including pads ($260 \times 180 \mu\text{m}^2$ excluding pads). Power consumption from a -3.3 V supply was less than 165 mW, and measured phase noise for the VCO at 1 MHz offset was -96.2 dBc/Hz.

Acknowledgments: This work was accomplished in the VLSI Research Group at the University of Toronto, Canada. The authors acknowledge the financial support of the University of Toronto and PMC-Sierra. The fabrications were carried out through the Canadian Microelectronics Corporation.

REFERENCES

1. Jung, B. & Harjani, R. (2004). A 20 GHz VCO with 5 GHz tuning range in 0.25 μm SiGe BiCMOS. ISSCC, Digest of Technical Papers, pp. 178-179.
2. Ettinger, K., Stelzer, A., Diskus, C. G. Thomann, W., Fenk, J. & Weigel, R. (2002). Single-chip 20-GHz VCO and frequency divider in SiGe technology. *IEEE Microwave Symposium, Digest*, Vol. 2, pp. 835-838.
3. Adler, R. (1973). A study of locking phenomena in oscillators. *Proceedings of the IRE*, Vol. 34, pp. 351-357, June 1946; Reprinted *Proc. IEEE*, Vol. 61, No. 10, pp. 1380-1385.
4. Kurokawa, K. (1973). Injection locking of microwave solid-state oscillators. *Proc. IEEE*, Vol. 61, pp. 1386-1410, Oct. 1973.
5. Djahanshahi, H., Saniei, N., Voinigescu, S. P., Maliepaard, M. C. & Salama, C. A. T. (2001). 20-GHz InP-HBT voltage-controlled oscillator with wide tuning range. RFIC Symposium, Digest, phoenix, Arizona, USA, pp. 161-164.
6. Jalali, B. & Pearton, S. J. (1995). *InP HBTs: Growth, processing and applications*. Artech House Inc., M.A.
7. Sakinger, E. (2005). *Broadband circuits for optical fiber communication*. Wiley Inc., N.J.
8. Saniei, N., Djahanshahi, H. & Salama, C. A. T. (2003). 25 GHz inductorless VCO in a 45 GHz SiGe technology. *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, Philadelphia, Pennsylvania, USA, pp. 269 -272.
9. Schuegraf, K., Racanelli, M., Kalburge, A., Shen, B., Hu, C., Chapek, D., Howard, D., Quon, D., Feiler, D., Domisch, D., U'Ren, G., Abdul-Ridha, H., Jie, Z., Jinshu, Z., Bell, K., Ring, K., Yin, K., Joshi, P., Akhtar, S., Lee, T. & Kempf, P. (2001). 0.18 μm SiGe BiCMOS technology for wireless and 40 Gb/s communication products. *Bipolar/BiCMOS Circuits and Technology Meeting, Proceedings*, pp. 147-1501.
10. Gilbert, B. (1975). Translinear circuits: A proposed classification. *Electronic letters*, Vol. 11, No. 1, pp. 14-16.
11. Saniei, N. (2005). A 20 GHz SiGe-HBT phase locked loop (PLL) for serial link applications. Ph.D. Thesis, University of Toronto.
12. Kinget, P., Melville, R., Long, D. & Gopinathan, V. (2002). An injection-locking scheme for precision quadrature generation. *IEEE J. Solid-State Circuits*, Vol. 37, No. 7, pp. 845-851.