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Design and Implementation of a Constant Frequency Sliding Mode Controller for a Luo Converter

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ABSTRACT

In this study, a robust controller for voltage regulation of a POESLL converter operated in continuous conduction mode is presented. The POESLL converter is a DC/DC converter with a high voltage gain. DC/DC converters are used in telecommunication systems, power sources and industrial applications. Owing to the switching operation, the structure of the POESLL converter is non-linear. In addition, because of the load and input voltage variations, the structure of the POESLL converter is time-varying. In order to regulate the output voltage of the POESLL converter, a non-linear controller is required. The proposed controller is developed based on constant frequency sliding mode method. The sliding mode controllers can cope with the non-linear and time-varying structure of the DC/DC converters. The performance of the proposed controller is studied in PSIM software. A laboratory model of the proposed controller has been implemented. In this paper, design, simulations and experimental results are presented to show the effective performance of the proposed controller for voltage regulation of the POESLL converter.

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1. INTRODUCTION

Nowadays, DC/DC converters are widely used in industrial applications [1, 2]. Theoretically, the conventional DC/DC converters such as boost, cuk, buck-boost, zeta and sepic can be used to increase the output voltage. However, in practical conditions, the voltage gain of the DC/DC converters is limited because of the parametric effects and inductor coil saturation. In addition, high increment in the output voltage increases switching losses.

The super lift (SL) method has been widely used in the design of DC/DC converters [3]. In this method, voltage gain of DC/DC converter increases in geometric progression. The positive output elementary super lift Luo (POESLL) converter has been designed based on super lift method. The POESLL converter is an attractive topology with a high voltage gain. In the same operating conditions, the inductor average current of the POESLL converter is less than the inductor average current of other conventional DC/DC converters. The inductor current is limited because of the inductor coil saturation problem. Therefore, the POESLL converter is a suitable candidate for power systems. The structure of the POESLL converter is non-linear and time-varying. To overcome these problems, a non-linear controller with robust performance is needed.

The signal flow graph (SFG) method has been widely used for modeling DC/DC converters [4, 5]. The design based on SFG method is simple; however, some dynamic characteristics are averaged out in the model of DC/DC converter. It attenuates the performance of the converter against parametric variations. The small signal sliding mode method for DC/DC converters has been introduced in [6]; however, this controller is designed in a specific operating point.

Design and implementation of proportional integral controllers and proportional integral divertive controllers have been reported in [7-10]. These controllers are sensitive against input voltage and load variations. The non-linear controllers possess many advantages compared with linear controllers. These are appropriate for large signal models. Based on such models, many non-linear techniques have been presented, for example, feedback linearization [11] and

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backstepping methods [12]; However, implementation of these controllers may be expensive and complicated. The sliding mode controller (SMC) is a type of non-linear controller. It is used for both linear and non-linear systems [13]. This control ensures stability of the POESLL converter in a wide range of operating conditions. In addition, the implementation of SMC is simple compared with other non-linear controllers. It is shown that the SMC is a possible solution for enhancing the performance of DC/DC converters [14, 15].

The traditional SMCs are developed by applying the hysteresis method (HM) [16-18]. In [19], a HM based SMC has been presented for output voltage regulation of the POESLL converter. In [20], current control for paralleled POESLL converters using HM based SMC has been introduced. In [21], a fuzzy logic controller-HM based SMC has been reported for DC/DC converters. These studies have shown the robust performance of the SMC; however, the HM based SMC has a major disadvantage. In this method, the switching frequency of DC/DC converter is variable, because of the hysteresis modulation. The variable frequency will result in noise and electromagnetic interference problems, inductor losses and large switching losses. In addition, it makes the design of the input and output filters more complicated. The constant frequency sliding mode method has been presented [22-24], which has these major disadvantages: difficulty in design and implementation and requiring more sensors and more calculations.

In this paper, design and implementation of a constant frequency SMC for a POESLL converter operated in continuous conduction mode are presented. This method is developed based on the equivalent control approach. In this method, an appropriate sliding surface S is defined. Then, an equivalent control law u_{eq} is derived in terms of the state variables of the converter by solving $\dot{S}=0$. Consequently, the defined sliding surface is indirectly enforced to reach the origin (S=0). In practice, in the implementation of the constant frequency sliding mode controller, the control law u_{eq} is constructed using a pulse width modulator. In this paper, the model of POESLL converter is derived. Then, the constant frequency SMC is designed. The performance of the proposed controller for POESLL converter is studied in different operating conditions. The analogue implementation of the proposed system is a useful contribution for researchers. The design of the constant frequency sliding mode controller is done using the reduced order equations of the POESLL converter. The advantages of this method are: less computations and less number of sensors [25].

This paper is organized as follows: In section 2, the average model of POESLL converter is derived and the performance of the converter is studied. In section 3, design of the proposed controller is done. The simulations and experimental results of the proposed system at various operating points are discussed in section 4. Finally, the conclusions are listed in section 5.

2. MODEL OF A POESLL CONVERTER IN CONTINUOUS CONDUCTION MODE

The diagram of the POESLL converter is shown in Figure 1(a). The output voltage increment can be performed by controlling the duty cycle of the switch. The POESLL converter is constituted of two diodes D_1, D_2, two capacitors C_1, C_2, inductor L and power switch Q. In Figure 1(a), R and E are load and input voltage, respectively. i_L is inductor current, v_{C1} capacitor (C_1) voltage and v_O is output voltage. It is supposed that the POESLL converter operates in continuous conduction mode and components of the converter are ideal. The circuit operation of the POESLL converter is studied in two conditions: The switch-ON condition and the switch-OFF condition. Figures 1(b) and (c) show these two conditions.

In switch-ON state, diode D_1 and switch conduct. Diode D_2 is OFF. The inductor current (i_L) is charged with slope E/L and capacitor C_1 is charged by input voltage. The load energy is provided by output capacitor.

In switch-OFF state, diode D_1 and switch are OFF and diode D_2 conducts. The inductor current is discharged with slope ($2E-v_O$)/L. In this state, inductor L and capacitor C_1 provide the output energy. The capacitor voltage v_{C1} is fixed with the assumption that the capacitor value C_1 is large enough. Therefore, the following relation is obtained for all times:

$$v_{C1}(t) = \mathrm{E} \tag{1}$$

Using (1), the averaged model of the POESLL converter is expressed as (2).

$$\begin{cases} L\dfrac{di_L}{dt} = E + (1-u)(E - v_O) \\ C_2\dfrac{dv_O}{dt} = (1-u)\, i_L - G v_O \end{cases} \tag{2}$$

where u ε (0, 1)

3. COMPARISION BETWEEN THE POESLL CONVERTERAND OTHER CONVENTIONAL CONVERTERS

In this section, the inductor average current of the POESLL converter is compared with the inductor average current of other conventional converters such as boost, cuk, buck-boost, sepic and zeta. This comparison is useful, because of the inductor losses problem. The inductor average current of the POESLL is obtained as:

$$I_L = \frac{I_{in}}{2-u} \tag{3}$$

In ideal conditions, $P_O=P_{in}$ then the relation between inductor average current and output average current is:

$$P_{in} = P_o \rightarrow EI_{in} = V_O I_O \rightarrow \frac{I_L}{I_O} = \frac{V_O}{E\ \ 2-u} = G-1 \tag{4}$$

where $G=V_O/E$ in steady state region.
The relation between inductor average current and output average current for other conventional DC/DC converters is obtained as (5).

$$\begin{cases} \dfrac{I_L}{I_O} = G & For\ \ Boost, Cuk, Sepic, Zeta \\ \dfrac{I_L}{I_O} = G+1 & For\ \ \text{Buck-boost} \end{cases} \tag{5}$$

A plot of I_L/I_O versus G is shown in Figure 2. It is clear that the inductor average current of the POESLL converter is less than that of other converters.

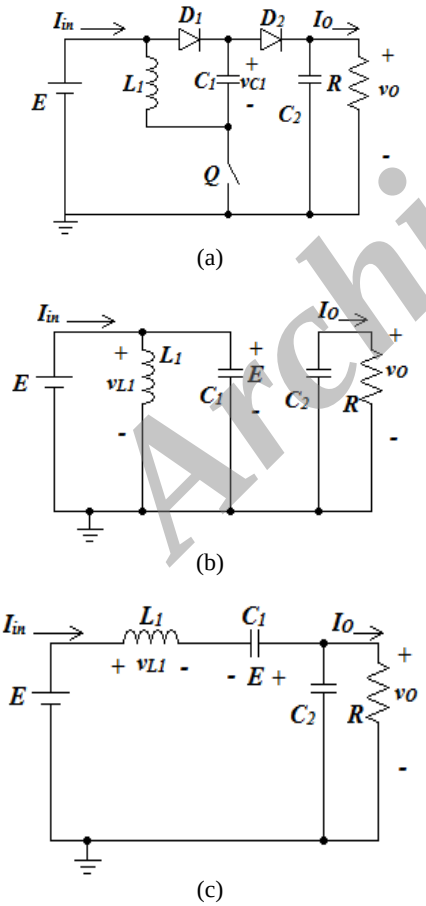


Figure 1. Diagram of the POESLL converter (a) Topology of the POESLL converter (b) POESLL converter in switch-ON condition (c) POESLL converter in switch-OFF condition

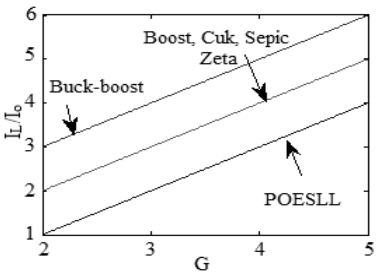


Figure 2. Plot of I_L/I_O versus G for DC/DC converters

4. DESIGN OF CONSTANT FREQUENCY SMC FOR THE POESLL

The SMC is flexible in design and simple in implementation. All the state variables of the converter can be sensed to generate the sliding surface, which enhance the performance of the SMC; however, this method makes the design of the controller more complicated [22-24]. It is worthwhile to note that complexity in the design of the sliding mode controller can be reduced by selecting a proper sliding surface. In this paper, the reduced order model of the converter is used to design the SMC. Therefore, only i_L and v_O are sensed to generate sliding surface. These variables are sufficient to regulate the output voltage of the converter. Here, the sliding surface of the POESLL converter is expressed as:

$$S = ai_L + bv_O + c\int\ \ \beta v_O - V_d \tag{6}$$

where a, b, c are controller parameters, V_d is the output voltage reference and β is a positive constant. In steady state region, $\beta V_O=V_d$. The presence of integral term of the output voltage reduces the output voltage error in steady state region [7]. Using Equations (2) and (6), the derivative of the sliding surface is obtained as:

$$\dot{S} = \frac{aE}{L} + \frac{a\ \ 1-u\ \ \ E-v_O}{L} + \frac{bi_{C2}}{C_2} + c\ \ \beta v_O - V_d \tag{7}$$

The equivalent control law is obtained by solving $\dot{S}=0$. It can be written as:

$$u_{eq} = \frac{k_1\ \ 2E-v_O\ \ + k_2 i_{C2} + k_3\ \ \beta v_O - V_d}{k_1\ \ E-v_O} \tag{8}$$

where:

$$k_1 = \frac{a}{L}, k_2 = \frac{b}{C_2}, k_3 = c \tag{9}$$

It can be seen that the output voltage and output capacitor current appear in equivalent control law u_{eq}. Therefore, these variables must be sensed to generate the equivalent control law. According to sliding mode theory, three conditions must be checked to ensure the

stability of the closed loop system: eexistence condition, reaching condition, stability condition {Tan, 2007 #23;Tan, 2008 #25;He, 2010 #26}.

4. 1. Existence Condition This condition ensures the existence of the sliding mode operation. The existence condition determines the acceptable range of the controller coefficients. This condition guarantees that all phase trajectories of the controller in the phase portrait are directed toward the sliding surface. It is expressed as Equation (10).

$$\begin{cases} \lim_{S\to 0^-} \dot{S} > 0 \\ \lim_{S\to 0^+} \dot{S} < 0 \end{cases} \tag{10}$$

when $\dot{S} > 0$, S<0, u=1 then:

$$\dot{S} = \frac{aE}{L} + \frac{bi_{C2}}{C_2} + c\ \ \beta v_O - V_d\ \ > 0 \tag{11}$$

when $\dot{S} < 0$, S>, u=0 then:

$$\dot{S} = \frac{aE}{L} + \frac{a\ \ E - v_O}{L} + \frac{bi_{C2}}{C_2} + c\ \ \beta v_O - V_d\ \ < 0 \tag{12}$$

The existence condition is expressed as:

$$\begin{cases} \dfrac{2aE_{\max}}{L} - \dfrac{av_{omax}}{L} + \dfrac{bi_{C2\max}}{C_2} + c\ \ \beta v_{Omax} - V_d\ \ < 0 \\ \dfrac{aE_{\min}}{L} + \dfrac{bi_{C2\min}}{C_2} + c\ \ \beta v_{Omin} - V_d\ \ > 0 \end{cases} \tag{13}$$

4. 2. Reaching Condition This condition guarantees that all the state variables of the system reach the origin (S=0) from any initial condition.

$$\begin{cases} \lim_{t\to\infty} \dot{S}\big|_{u=0} < 0 \\ \lim_{t\to\infty} \dot{S}\big|_{u=1} > 0 \end{cases} \tag{14}$$

This condition is satisfied by appropriate selection of the controller coefficients shown in (13) using the existence condition.

4. 3. Stability Condition The stability condition ensures that the states errors of the POESLL converter are kept on the origin (S=0). For the constant frequency SMC, this condition is checked by determining the state space equations of the closed loop system and then small signal analysis around their equilibrium points.

4. 3. 1. State Space Equations of the Closed Loop System The dynamic equations of the POESLL converter under the constant frequency SMC are obtained by replacing u_{eq} in (2) with (8) which yields:

$$\begin{cases} L\dfrac{di_L}{dt} = E - \dfrac{k_1E + k_2i_{c2} + k_3\ \ \beta v_O - V_d}{k_1\ \ E - v_O}\ \ E - v_O \\ C_2\dfrac{dv_o}{dt} = -\dfrac{k_1E + k_2i_{c2} + k_3\ \ \beta v_O - V_d}{k_1\ \ E - v_O} i_L - \dfrac{v_O}{R} \end{cases} \tag{15}$$

4. 3. 2. Equilibrium Points of the POESLL Converter Suppose that all conditions are satisfied. In origin (S=0), all the state variables of the converter reach the equilibrium points; that is, $dv_O/dt=di_L/dt=0$. Then, the equilibrium points of the converter are expressed as:

$$\begin{cases} \mathrm{V_O} = \dfrac{\mathrm{V_d}}{\beta} \\ \mathrm{I_L} = \dfrac{\mathrm{V_d}\ \ \mathrm{V_d} - \mathrm{E}}{\mathrm{RE}} \end{cases} \tag{16}$$

In (16), V_O, V_d and I_L are output voltage, voltage reference and inductor current in steady state region, respectively. R and E are output resistance and input voltage.

4. 3. 3. Small Signal Analysis of the Dynamic Equations Equation (15) can be expressed as (17). By using the following static condition $\beta V_O - V_d = 0$ and the assumption $V_O >> V_d$; then, the linearized equations of the closed loop system can be given as (18).

$$\begin{cases} \mathrm{L}\dfrac{\mathrm{d}\ \ \mathrm{I_L} + \mathrm{i_L}}{\mathrm{dt}} = \mathrm{E} - \dfrac{\mathrm{a_1E} + \mathrm{a_2}\ \ \alpha(\mathrm{V_O} + \mathrm{v_O}\ \ - \mathrm{v}_d)}{\mathrm{a_1}} \\ \quad - \dfrac{\mathrm{a_3}\int\ \ \alpha\ \ \mathrm{V_O} + \mathrm{v_O}\ \ - \mathrm{v}_d\ \ \mathrm{dt} + \mathrm{a_4C_2d}\ \ \mathrm{V_O} + \mathrm{v_O}\ \ / \mathrm{dt}}{\mathrm{a_1}} \\ \mathrm{C_2}\dfrac{\mathrm{d}\ \ \mathrm{V_O} + \mathrm{v_O}}{\mathrm{dt}} = \dfrac{-\mathrm{a_1E} - \mathrm{a_2}\ \ \alpha(\mathrm{V_O} + \mathrm{v_O}\ \ - \mathrm{v}_d)}{\mathrm{a_1}\ \ \mathrm{E} - \mathrm{V_O} - \mathrm{v_O}} \\ - \dfrac{\mathrm{a_3}\int\ \ \alpha\ \ \mathrm{V_O} + \mathrm{v_O}\ \ - \mathrm{v}_d\ \ \mathrm{dt} + \mathrm{a_4C_2d}\ \ \mathrm{V_O} + \mathrm{v_O}\ \ / \mathrm{dt}}{\mathrm{a_1}\ \ \mathrm{E} - \mathrm{V_O} - \mathrm{v_O}} - \dfrac{\mathrm{V_O} + \mathrm{v_O}}{\mathrm{R}} \end{cases} \tag{17}$$

$$\begin{cases} \dfrac{\mathrm{d\,i_L}}{\mathrm{dt}} = \mathrm{b_{11}i_L} + \mathrm{b_{12}v_O} \\ \dfrac{\mathrm{d\,v_O}}{\mathrm{dt}} = \mathrm{b_{21}i_L} + \mathrm{b_{22}v_O} \end{cases} \tag{18}$$

where:

$$\begin{aligned} b_{11} &= \frac{k_2E}{L\ \ E - V_d\ \ \left(k_1 - \frac{k_2V_d}{RE}\right)} \\ b_{12} &= -\frac{k_3\beta}{Lk_1} - \frac{k_2\ \ 2V_d - E}{L\ \ E - V_d\ \ \left(k_1 - \frac{k_2V_d}{RE}\right)R} - \frac{k_3k_2\beta V_d}{Lk_1\ \ k_1 - k_2V_d / \ RE\ \ \ RE} \\ b_{21} &= -\frac{k_1E}{C_2\ \ E - V_d\ \ \ k_1 - k_2V_d / \ RE} \\ b_{22} &= \frac{k_1\ \ 2V_d - E}{C_2\ \ E - V_d\ \ \ k_1 - k_2V_d / \ RE\ \ \ R} \end{aligned} \tag{19}$$

The characteristics equation of the linearized closed loop system is written as Equation (20).

$$\begin{vmatrix} S-b_{11} & -b_{12} \\ -b_{21} & S-b_{22} \end{vmatrix} = S^2 + d_1 S + d_2 = 0 \quad (20)$$

where:

$$d_1 = -b_{11} - b_{22}, d_2 = b_{11}b_{22} - b_{12}b_{21} \quad (21)$$

According to Routh criterion, the following conditions must be satisfied to ensure the closed loop stability of the linearized system.

$$d_1 > 0, d_2 > 0 \quad (22)$$

By mathematically solving Equation (19) and replacing into Equation (22), the stability of the closed loop system is determined; then, by using Equation (13) and observing the output voltage response, the proper range of the controller coefficients can be given.

5. SIMULATION AND EXPERIMENTAL RESULTS

In this section, simulations and experimental results are presented to show the effectiveness of the proposed sliding mode controller for a POESLL converter operated in continuous conduction mode. The coefficients of the proposed controller are selected as: k_1=0.015, k_2=0.02, k_3=0.1, β=0.1. The circuit parameters of the POESLL converter are listed in Table 1. The simulations have been performed in PSIM software. The circuit elements of the converter are listed in Table 2.

The laboratory model of the POESLL converter under the proposed controller is shown in Figure 3. The proposed system has been implemented in analogue platform. From Figure 3, it can be seen that the equivalent control law is implemented using Op- Amps; then, it is compared with a saw tooth waveform to generate the switching signal. The obtained signal is given to the switch (MOSFET) using an optocoupler (TLP250).

5. 1. Simulations Results Figure 4 shows the transient behaviour of the output voltage of the POESLL converter for E=9V and R=50, 100 Ω. Figure 5 shows the transient behaviour of the output voltage of the POESLL converter for E=12V and R=50, 100 Ω. From Figures 4 and 5, it can be seen that the voltage of the converter under the proposed controller has a quick settling time and small overshoot.

Figure 6 depicts the behavior of the output voltage of the POESLL converter for E=9 V and load change between 50 and 100 Ω. It is clear that the voltage of the POESLL converter under the proposed controller has a small overshoot and quick settling time. Figure 7 shows the response of the output voltage of the POESLL converter for E=12 V and load change between 100 Ω and 50 Ω. It can be seen that the output voltage of the POESLL converter under the proposed controller has a small overshoot and quick settling time.

TABLE 1. Parameters of the converter

Name	Symbol	Value
Output voltage	V_O	30V
Reference voltage	V_d	3V
Input voltage	E	9, 12V
Inductor	L	0.0004H
Capacitor	C_1, C_2	0.0001F
Output resistance	R	50Ω to 100Ω
Frequency switching	F	20kHz
Equivalent series resistor of inductor	ESRL	0.35Ω
Equivalent series resistor of capacitor	ESRC	.02Ω

TABLE 2. Elements of the converter

Name	Type
Switch	IRFZ470
Diode	1N555
Capacitor	0.0001F/100V(electrolytic)
Inductor	4×0.0001H/5A
Op Amp	LF351

5. 2. Experimental Results Figure 8 shows the experimental response of the voltage for E=9 V and load change between 50 Ω and 100 Ω. Figure 9 shows the experimental behaviour of the voltage for E=12 V and load change between 50 Ω and 100 Ω. It is clear that the closed loop system is stable in different operating conditions.

Figures 8 and 9 demonstrate the effectiveness of the POESLL converter under the proposed controller. Figures 10.a and b show the output voltage, switching signal and inductor current of the POESLL converter in steady state region for E=9V and R=50Ω and V_O=30 V. Figures 11.a and b show the output voltage and switching signal and inductor current of the POESLL converter in steady state region for E=12V and R=100Ω and V_O=30 V.

Figure 12 depicts the response of the voltage of the POESLL converter for E=9 V and R=50 Ω and voltage change between 18 and 30 V.

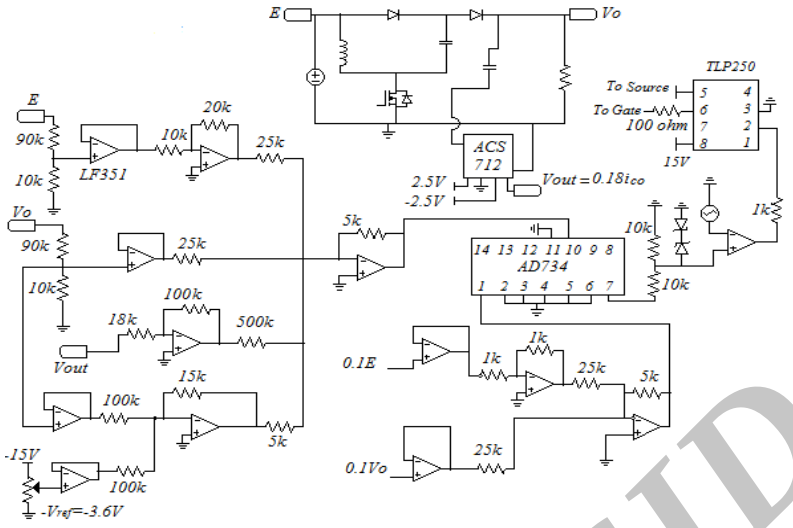


Figure 3. Laboratory model of the POESLL converter under the constant frequency SMC

Figure 13 depicts the response of the voltage of the POESLL converter for E=12 V and R=100 Ω and voltage change between 30 V and 42 V.

Figure 14 shows the laboratory model of the proposed system in analogue platform.

In summary, from Figures 10 and 11, it is found that the switching frequency is 20 kHz and the POESLL works in continuous conduction mode. Moreover, the simulation results of the POESLL converter under the proposed controller match the experimental results with a maximum tolerance of 1%.

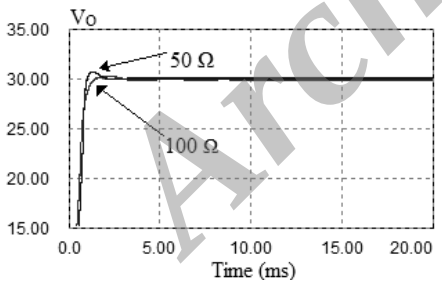


Figure 4. Transient behaviour of the output voltage for E=9 V

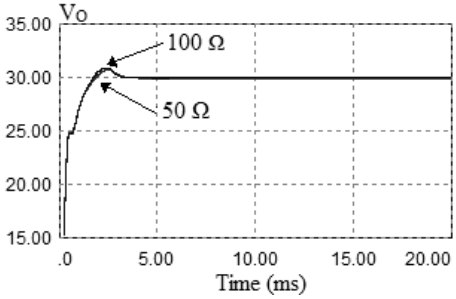


Figure 5. Transient behaviour of the output voltage for E=12V

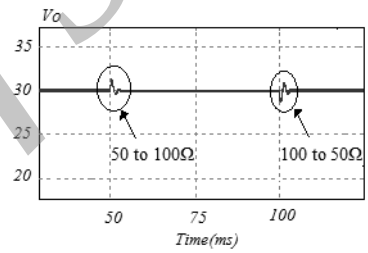


Figure 6. Output voltage of the POESLL converter for E=9 V and load variations between 50 and 100 Ω

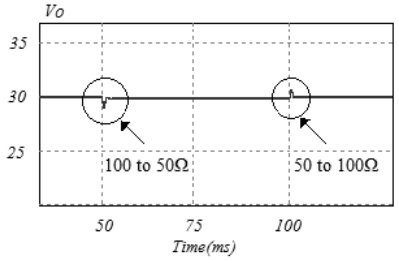


Figure 7. Output voltage of the POESLL converter for E=12 V and load variations between 100 and 50 Ω

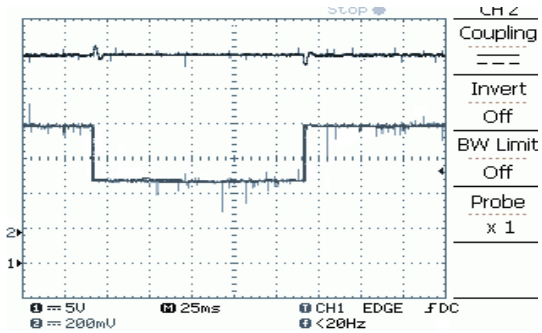


Figure 8. Experimental result for load change and E=9 V [Ch1:5V/Div-output voltage, Ch2:200mV/Div-load]

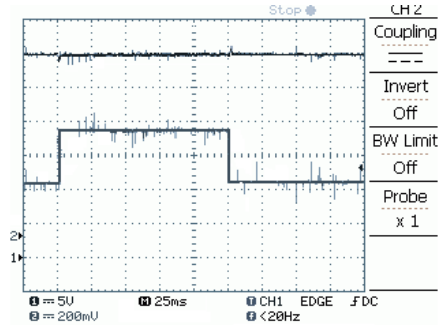
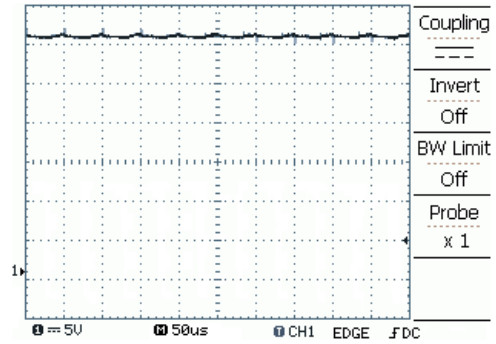
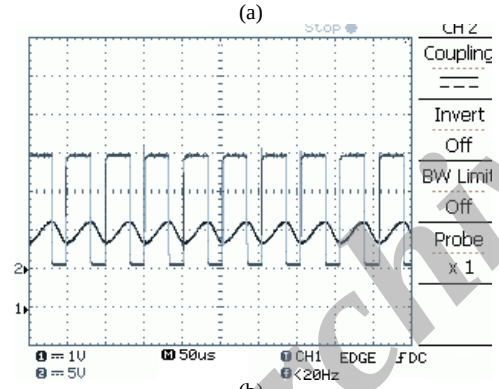


Figure 9. Experimental result for load variation and E=12V [Ch1:5V/Div-output voltage, Ch2:200mV/Div-load]

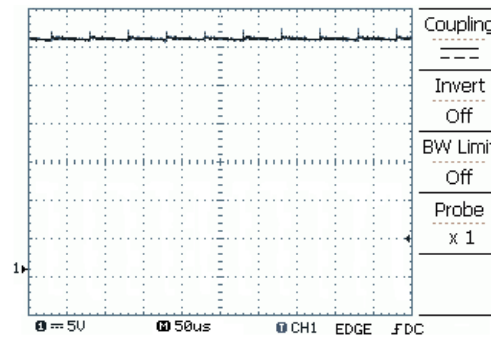


(a)

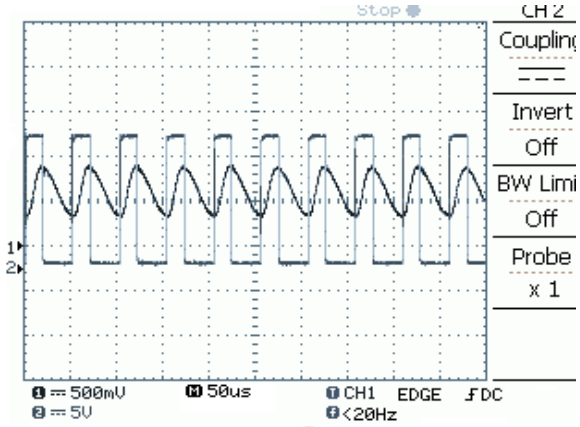


(b)

Figure 10. Experimental response of the output voltage of the POESLL converter for E=9 V and R=50 Ω in steady state region; (a) Response of the output voltage [Ch1:5 V/Div-output voltage] (b) Response of the switching signal and inductor current [Ch1:1 V/Div-inductor current and Ch2:5 V/Div-switching signal]



(a)



(b)

Figure 11. Experimental response of the output voltage of the POESLL converter for E=12V and R=100 Ω in steady state region (a) Response of the output voltage [Ch1:5 V/Div-output voltage] (b) Response of the switching signal and inductor current [Ch1:1 V/Div-inductor current and Ch2:5 V/Div-switching signal]

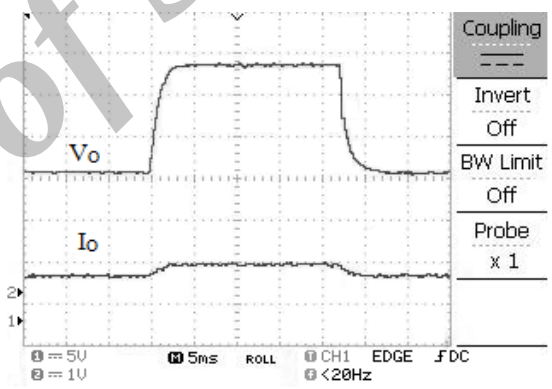


Figure 12. Experimental result for E=9 V and R=50 Ω and output voltage change between 30 V and 42 V[Ch1:5V/Div-output voltage and Ch2:1V/Div-load]

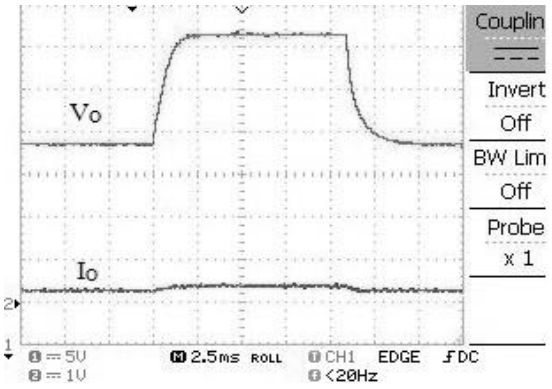


Figure 13. Experimental result for E=12 V and R=100 Ω and output voltage change between 30 and 42 V [Ch1:5V/Div-output voltage and Ch2:1V/Div-load] output voltage and Ch2:1V/Div-load]

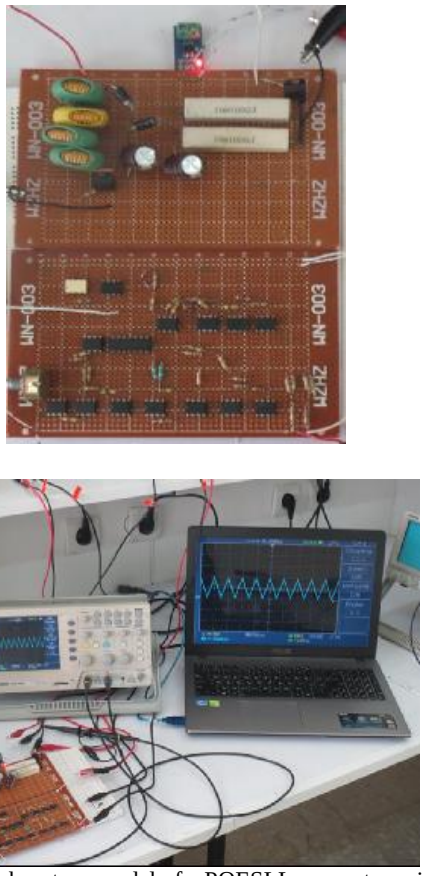


Figure 14. Laboratory model of a POESLL converter using a constant frequency SMC

6. CONCLUSIONS

In this paper, the design of a constant frequency SMC for output voltage regulation of the POESLL has been successfully presented. The constant frequency sliding mode control scheme has been implemented. The proposed controller ensures robustness and stability against load and input voltage variations compared with linear controllers. Simulation and experimental results are presented to show the performance of the proposed controller. The proposed controller is suitable for most commercial applications. The advantages of the proposed controller implemented in this paper are: constant frequency, simple implementation, robustness performance against load and voltage variations and less number of sensors.

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Design and Implementation of a Constant Frequency Sliding Mode Controller for a Luo Converter

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چکیده

در این مقاله، یک کنترل‌کننده‌ی مقاوم برای تنظیم ولتاژ مبدل POESLL در حالت هدایت پیوسته معرفی شده است. مبدل POESLL یک مبدل DC/DC با بهره‌ی انتقال ولتاژ بالاست. از این مبدل می‌توان در منابع توان ثابت، سیستم‌های مخابراتی و کاربردهای صنعتی استفاده کرد. به خاطر عملکرد کلیدزنی، ساختار مبدل POESLL غیرخطی است. علاوه بر این، به خاطر نوسانات بار و ولتاژ ورودی، ساختار این مبدل متغیر با زمان است. به منظور بهبود عملکرد و تنظیم ولتاژ خروجی، مبدل نیاز به یک کنترل‌کننده‌ی مقاوم دارد. کنترل‌کننده‌ی پیشنهادشده در این مقاله بر اساس روش کنترل مد لغزشی فرکانس ثابت طراحی می‌شود. کنترل‌کننده‌های مد لغزشی متناسب با ساختار غیرخطی و متغیر با زمان مبدل‌های DC/DC هستند. عملکرد کنترل‌کننده‌ی پیشنهادشده در این مقاله در نرم‌افزار PSIM بررسی شده است. علاوه بر این، یک نمونه از آن ساخته شده است. در این مقاله، طراحی، شبیه‌سازی و نتایج عملی ارائه می‌شوند تا عملکرد مؤثر کنترل‌کننده پیشنهادی برای تنظیم ولتاژ خروجی مبدل POESLL را نشان دهند.

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