IJE TRANSACTIONS B: Applications Vol. 31, No. 5, (May 2018) 699-704

International Journal of Engineering

Journal Homepage: www.ije.ir

A New Circuit Scheme for Wide Dynamic Circuits

M. Asyaei*

School of Engineering, Damghan University, Damghan, Iran

PAPER INFO

Paper history:
Received 06 November 2017
Received in revised form 07 December 2017
Accepted 16 Januray 2018

Keywords:
Dynamic circuit
Keeper
Leakage current
Noise immunity
Wide fan-in gates

ABSTRACT

In this paper, a new circuit scheme is proposed to reduce the power consumption of dynamic circuits. In the proposed circuit, an NMOS keeper transistor is used to maintain the voltage level in the output node against charge sharing, leakage current and noise sources. Using the proposed keeper scheme, the voltage swing on the dynamic node is lowered to reduce the power consumption of wide fan-in gates. Furthermore, the subthreshold leakage current is decreased by using the footer transistor in diode configuration and consequently, the noise immunity is increased in the proposed circuit. Simulation results of wide fan-in OR gates in 90nm CMOS technology demonstrate 48% power reduction and 1.65× noise-immunity improvement at the same delay compared to the conventional dynamic circuit for 32-bit OR gates.

***doi**: 10.5829/ije.2018.31.04a.03*

NOMENCLATURE

UNA	Unity noise average	t_p	Delay
FOM	Figure of merit	P_t	Total power consumption

1. INTRODUCTION

Dynamic circuits are preferred as compared to static ones due to their advantages including high speed, low transistor count and reduced load capacitance [1]. However, dynamic circuits suffer from some drawbacks such as lower noise immunity and higher power consumption in comparison with static ones.

On the other hand, as the technology scaled down, the supply voltage and the threshold voltage (V_{TH}) is scaled down to achieve low power consumption and high performance[2-4]. Reducing the threshold voltage increases the subthreshold leakage current exponentially and hence the noise immunity is degraded especially for wide fan-in gates.

Wide fan-in gates are mainly used in high-performance applications such as read-out paths of multiport memories, L1 caches, match lines of ternary content addressable memories (TCAMs), tag comparators, programmable logic arrays (PLAs), and wide multiplexers (MUXs). Therefore, improving the noise immunity, power consumption and performance of the wide gates are of major issues in the modern technologies.

To achieve the desired robustness, dynamic circuits employ keepers to maintain the state of the dynamic node during the evaluation phase, as shown in Figure 1. A conventional keeper is a PMOS pull-up transistor which compensates any voltage drop in the dynamic node due to the charge sharing, leakage current, and noise sources. However, the keeper transistor producesa large contention current during the evaluation phase and consequently increases the delay and power consumption. Besides these disadvantages, the conventional keeper cannot track process variations and the leakage currents in the pull-down network. Therefore, the conventional keeper limits the number of pull-down legs [5]. Keeper upsizing is a traditional way to achieve the desired noise immunity in recent technology generations, but the power consumption and delay are increased due to high current contention.

*Corresponding Author Email: *m.asyaei@du.ac.ir* (M. Asyaei)

Please cite this article as: M. Asyaei, A New Circuit Scheme for Wide Dynamic Circuits, International Journal of Engineering (IJE), IJE TRANSACTIONS B: Applications Vol. 31, No. 5, (May 2018) 699-704

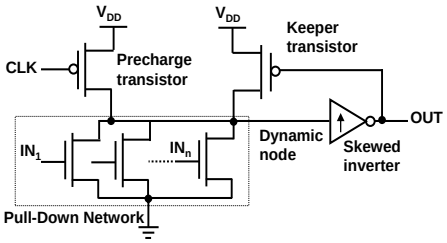

Figure 1. Conventional dynamic circuit

Thus, there is a trade-off between noise immunity and other design characteristics. Another issue is the leakage current which accounts for a significant portion of the total power consumption [6].

Several works have been presented in the literature to address the above-mentioned issues. The existing circuit techniques try to improve some of the design characteristics at the cost of degrading others. These circuits usually change the circuit topology of the evaluation network or the keeper scheme. Recently, some techniques have been proposed in the literature in which the evaluation network and the keeper circuit are restructured simultaneously to improve most of the characteristics [7-10].

This paper presents a new circuit structure for wide fan-in gates in which the traditional keeper is removed and a new keeper circuit scheme is employed to alleviate the contention. In fact, the evaluation circuit is modified to decrease the power consumption by lowering the voltage swing on the dynamic node. Furthermore, the noise immunity is increased due to the stacking effect.

The rest of the paper is arranged in the followingmanner. The proposed dynamic circuit is presented in Section 2. Simulation results and comparisons are explained in Section 3. Finally, the conclusion is drawn in Section 4.

2. PROPOSED DYNAMIC CIRCUIT

The main idea in the proposed circuit is that the traditional keeper is removed and a new keeper circuit scheme is used to reduce the voltage swing on the dynamic node. Since the voltage of the dynamic node is discharged to a non-zero voltage, the traditional output inverter is not applicable. This is due to the fact that when the voltage of the dynamic node is equal to a non-zero voltage, both PMOS and NMOS transistors in the output inverter are turned on simultaneously and hence the short circuit power is increased. For this reason, a new circuit scheme is needed to generate the output voltage, as illustrated in Figure 2.

As shown in Figure 2, both the evaluation network and keeper circuit are reconstructed. Noted the dynamic node is afloat in this circuit, but the voltage level of the output node is maintained by the keeper circuit including transistors M_2, M_3, M_4 and the NMOS keeper transistor M_N. Therefore, any unwanted discharging in the dynamic node cannot change the output level.

In The proposed dynamic circuit shown in Figure 2, transistor M_{Pre} is used to charge the dynamic node *Dyn* in the precharge phase. In addition, transistors M_1 and M_5 are employed to discharge nodes *foot* and *Out*, respectively, in this phase.

Transistors M_3 and M_4 are employed as an inverter in which the reference voltage (V_{Ref}) is used to supply the inverter. This inverter controls transistor M_N according to the voltage of node *foot*. Since maximum voltage established on node *foot* is lower than V_{DD}, V_{Ref} is used instead of V_{DD} for proper operation. In fact, the reference voltage is chosen such that transistor M_4 can be turned off when at least one conductive path exists in the pull-down network and the voltage of node *foot* is increased. Therefore, the value of V_{ref} is chosen between V_{DD} and V_{THP} (the threshold voltage of PMOS transistors).

The value of reference voltage directly affects the robustness and performance of the proposed circuit, thus the effect of process variation can be reduced using an appropriate reference circuit. To generate V_{Ref} in the proposed circuit, the used reference circuit is the same as presented by Asyaei and Ebrahimi [11]. This reference circuit properly tracks the process variations, as stated in the literature [11]. Therefore, the performance of the proposed circuit is improved without noise immunity degradation.

As shown in Figure 2, transistor M_2 is configured in the diode connection to achieve the following advantages. First, the voltage at the dynamic node cannot be reduced to the ground, thus the voltage swing across the pull-down network is decreased. As a result, the dynamic power consumption is reduced due to the direct relationship between the dynamic power consumption and voltage swing [1].

Second, the switching threshold voltage of the proposed circuit is two times of the threshold voltage of NMOS transistors due to the diode footer transistor M_1 [12].

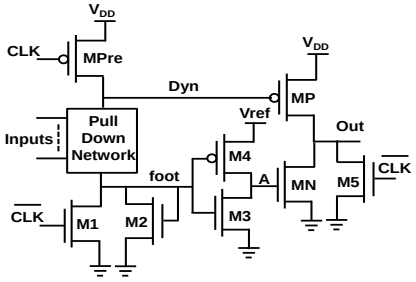

Figure 2. The proposed dynamic circuit

Therefore, the noise immunity is increased because of higher switching threshold voltage at the expense of speed degradation.

Third, the subthreshold leakage current is reduced because of the following reasons. 1) The threshold voltage of transistors in the pull-down network is increased due to the body effect. 2) The gate-source voltage of these transistors becomes negative due to some voltage drop on the node *foot*. 3) The drain-source voltage of transistors in the pull-down network is reduced due to this voltage drop.

In the proposed circuit, the voltage of node *Dyn* is charged to V_{DD} in the precharge phase and conditionally discharged to a non-zero voltage in the evaluation phase. Thus, in the proposed circuit like the conventional circuit, any noise source must be able to discharge node *Dyn* from V_{DD}. As a result, swing reduction does not degrade the noise immunity in comparison with other dynamic circuits. However, the minimum supply voltage is increased in the proposed circuit compared to the conventional circuit due to the lower voltage swing on node *Dyn*. For example, if node *Dyn* is discharged to $V_{DD}/2$, the minimum supply voltage would be $2V_{tp}$ which is needed to turn on transistor M_P.

Referring to the circuit schematic shown in Figure 2, two operating phases of the proposed circuit are described in detail as follows.

In the precharge phase, input and clock signals are in the low level (CLK='0' in Figure 2). Therefore, transistors M_{Pre}, M_1, M_4, M_5 and M_N are ON and transistors M_2, M_3 and M_P are OFF. Therefore, the dynamic node *Dyn* is charged to V_{DD} via transistor M_{Pre} and node *A* is charged to V_{ref} through transistor M_4. Also, transistors M_1 and M_5 will discharge nodes *foot* and *Out* to the ground, respectively. Since V_{ref} is lower than V_{DD}, the conductance of transistor M_N is not enough to discharge the load capacitance on the output node. Thus transistor M_5 is necessary to reduce the high to low transition time. In addition, transistor M_1 is required to discharge node *foot*; otherwise, the wrong output may be generated due to charging this node in the previous clock cycles.

In the evaluation phase, the clock signal is high (CLK='1' in Figure 2) and input signals can be high. Therefore, transistors M_{Pre}, M_1 and M_5 are OFF. Transistors M_2, M_3 and M_P become ON or OFF according to the input signals. Two states may happened depending on the input signals. First, there is no conductive path in the pull-down network and the only current is the subthreshold leakage current. As mentioned earlier, the subthreshold leakage current is lowered because of three reasons. As a result, transistor M_N remains ON and keeps the output voltage level.

At the Second state, at least one conductive path is established across the pull-down network. Thus, nodes *Dyn* and *foot* are decreased and increased, respectively to reach the same non-zero voltage, as shown in Figure 3. Therefore, transistors M_3 and M_N are turned ON and OFF, respectively. In addition, transistor M_P is turned ON. Finally, the output voltage level become high.

4. SIMULATION RESULTS AND COMPARISONS

The studied circuits are simulated to compare with the proposed circuit (Figure 2). Simulations are done using HSPICE simulator in the GPDK 90nm CMOS technology model using the standard performance transistors. The power supply is set 1V and the hotspot temperature of 110ºC is used for simulations. In addition, the output capacitance load of 5fF is used in this paper.

The wide fan-in OR gates with 8, 16, 32, 64 inputs are designed using the studied techniques and the proposed circuit. Furthermore, simulations are performed using the simulation framework presented in[13]. These wide OR gates are designed to obtain the same propagation delay for a given input, i.e., 70, 80, 90, and 110 ps for 8, 16, 32 and 64-input OR gates, respectively.

For all circuits, the length of all transistors is set to the minimum size. The width of transistors in the pull-down network is set to the minimum width. The width of other transistors is initially set to the minimum size and it is necessarily changed to achieve the same delay for a given fan-in.

In the proposed circuit (Figure 3), the size of transistor M_P is changed to achieve the specific delay. Other transistors are set to the minimum size.

A comparison of the estimated area for 32-input OR gates is shown in Figure 4. The results are normalized to the consumed area of the conventional circuit. As it is shown, the proposed circuit and the conventional design have the smaller normalized area compared to other designs under the same delay, respectively.

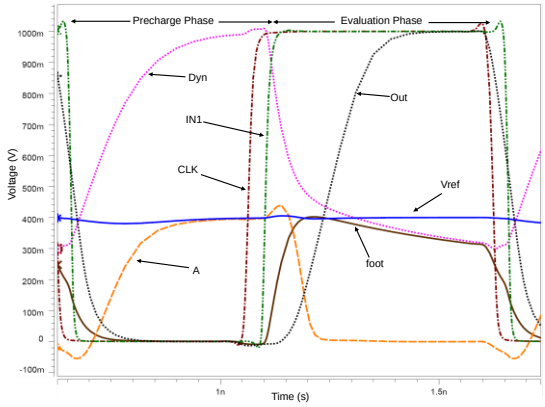

Figure 3. Waveforms of the proposed circuit

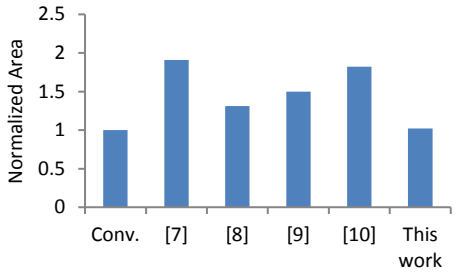

Figure 4. Comparison of the normalized estimated areaunder the same delay

To compare the noise immunity of the circuit techniques, a noise metric called the unity noise average (UNA) is used in this study. It is defined as the amplitude of the input noise causing the same voltage average at the output node [14]. This metric is expressed as:

$$UNA = \{V_{noise} : V_{noise_{Avg}} = V_{out_{Avg}}\} \quad (1)$$

To compare the UNA of the studied circuits, the amplitude of the input noise is varied until the voltage average of the output signal becomes equal to that of the input noise. To measure the UNA in the worst case, identical noise pulses are applied to all inputs of the OR gate.

Numerical results for normalized UNAs are listed in Table 1. Simulation results are normalized to the UNA of the conventional circuit to have a better comparison. In addition, all simulations are done in the same delay for a given fan-in, as mentioned earlier.

As seen in Table 1, UNA of the proposed circuit is higher than other studied circuits except for the circuit proposed in the literature [9]. Noted the proposed circuit suffers from the higher consumed area and static power consumption compared to the other proposed circuit. In the proposed circuit, noise immunity is increased due to the lower leakage current and higher switching threshold voltage in comparison with the conventional circuit, as stated in Section 3. Simulation results exhibit from 1.22 to 1.97 times improvement in noise immunity compared to the conventional design.

TABLE 1. Comparison of UNAs normalized to the conventional circuit under the same delay

Fan-in	Conv.	[7]	[8]	[9]	[10]	This work
8	1	1.51	1.09	1.64	1.69	1.22
16	1	1.69	1.21	1.87	1.46	1.44
32	1	1.79	1.29	2.12	1.64	1.65
64	1	1.86	1.59	2.31	1.79	1.97

A comparison of power consumption is shown in Figure 5. The obtained results are normalized to the power consumption of the conventional circuit.

Simulation results demonstrate a reduction in normalized power consumption from 48 to 52% compared to the conventional circuit. As shown in Figure 5, the proposed circuit has lower power consumption in comparison with other circuits.

To compare studied circuits with each other, a measurement of quality is required to account for noise immunity, delay, and power consumption together. A metric was defined in the literature [15] to consider the power-delay product (PDP) and noise immunity. Since the energy-delay product (EDP) is more important parameter rather than PDP, the EDP is used in the defined figure of merit (FOM). Since the EDP is equal to $P_t \times t_p^2$ [1], the time delay has squared to consider this parameter. Therefore, a figure of merit (FOM) is defined for the examined circuits as follows:

$$FOM = \frac{UNA_{norm}}{P_{t-norm} \times t^2_{P-norm}} \quad (2)$$

where UNA_{norm}, $t_{P\text{-}norm}$, and $P_{t\text{-}norm}$ are unity noise average, worst case delay and the total power consumption of the circuit, respectively. All design parameters are normalized to the conventional circuit counterparts to consider the improvements.

The FOM of the simulated circuits is illustrated in Figure 6. Simulations are performed for 32-input OR gate under the same delay. As shown in Figure 6, the proposed circuit achieved 3.17 times improvement in FOM compared to the conventional circuit.

In order to consider the effect of process variation on the proposed circuit, simulations are done on different process corners. The process corners include fast PMOS-fast NMOS (fPfN), slow PMOS-fast NMOS (sPfN), fast PMOS-slow NMOS (fPsN) and slow PMOS-slow NMOS (sPsN).

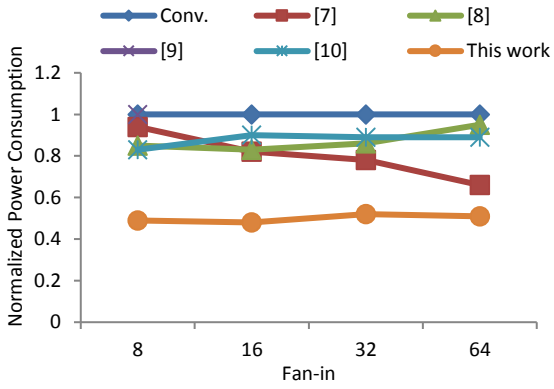

Figure 5. Comparison of the normalized power consumption under the same delay

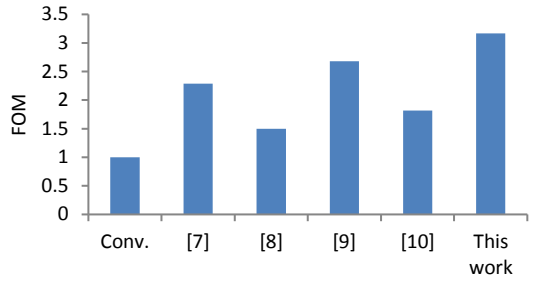

Figure 6. FOM of 32-input OR gates under the same delay

Simulation results for delay and power consumption of the proposed circuit at different process corners are illustrated in Figure 7. The delay and power consumption of the proposed circuit are normalized to those parameters in the typical process (i.e., typical PMOS-typical NMOS (tPtN)), as shown in Figure 7.

According to this figure, normalized delay and power consumption of the proposed circuit have lowervariations in sPfN, fPsN corners compared to the rest.

Furthermore, the proposed circuit is simulated at three temperatures and different supply voltages to consider voltage and temperature variation effects. Simulation results are shown in Figures 8 and 9 for several temperatures and supply voltages, respectively.

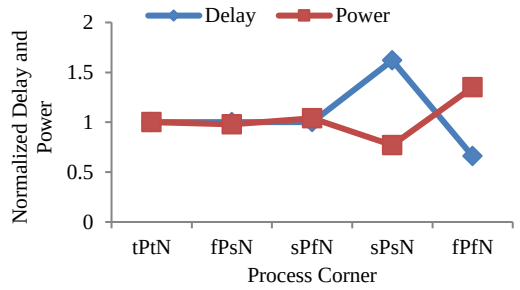

Figure 7. Process variation effects on the normalized delay and power of the proposed circuit

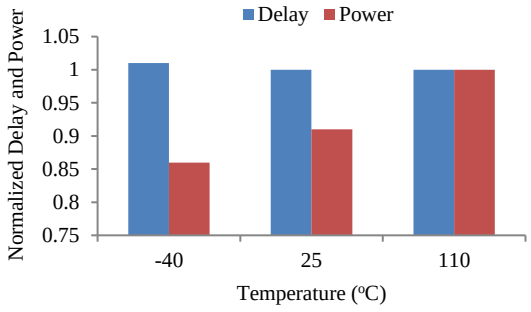

Figure 8. Temperature variation effects on the normalized delay and power of the proposed circuit

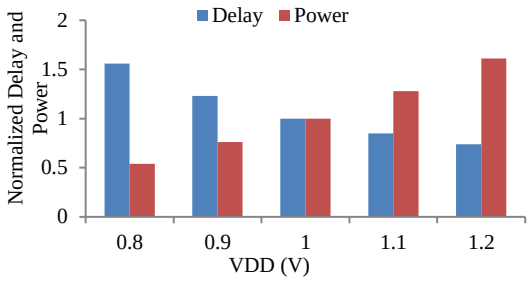

Figure 9. Voltage variation effects on the normalized delay and power of the proposed circuit

The delay and power consumption of the proposed circuitare normalized to those parameters at 1V in typical process at 110^0C. As shown in Figure 8, the normalized delay is slightly changed with the temperature variations in the proposed circuit.

According to the simulation results illustrated in Figures 7-9, the operation of the proposed circuit is not failed due to the process, voltage and temperature variations.

5. CONCLUSIONS

This paper introduces a new circuit scheme to improve the noise immunity and reduce the power consumption of wide fan-in gates in deep sub-micron CMOS technologies. To achieve these benefits, re-engineering of the conventional dynamic circuit is required. For this reason, the keeper circuit and the evaluation network are modified.

The main idea of the proposed circuit is based on the use of a footer transistor in a diode configuration to keep the voltage level of the output node against the noise sources. Moreover, the power consumption is decreased by reducing the voltage swing at the dynamic node. Besides, by employing the footer transistor, the subthreshold leakage current of wide fan-in gates is reduced because of the stacking effect. That results in more power reduction and noise immunity improvement.

Simulation results demonstrate that the proposed circuit has lower power consumption for wide fan-in gates compared to the conventional circuit. Thus, the proposed circuit is suitable to implement wide fan-in gates which are usually employed in high-speed applications like microprocessors.

6. REFERENCES

1. Rabaey, J.M., Chandrakasan, A.P. and Nikolic, B., "Digital integrated circuits, Prentice hall Englewood Cliffs, Vol. 2, (2002).

2. Niaraki, R. and Nobakht, M., "A sub-threshold 9t sram cell with high write and read ability with bit interleaving capability", ***International Journal of Engineering,Transactions B: Applications***, Vol. 29, No. 5, (2016), 630-636.
3. Ghorban, N.D.A., Navi, K. and Hashemipour, O., "High speed full swing current mode bicmos logical operators", ***International Journal of Engineering***, ***Transaction A: Basics***, Vol. 20, No. 3, (2007), 211-220.
4. Juneja, K., Singh, N. and Sharma, Y., "High-performance and low-power clock branch sharing pseudo-nmos level converting flip-flop", ***International Journal of Engineering***, ***Transaction C: Aspects***, Vol. 26, No. 3, (2013), 315-322.
5. Jeyasingh, R.G.D., Bhat, N. and Amrutur, B., "Adaptive keeper design for dynamic logic circuits using rate sensing technique", ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems***, Vol. 19, No. 2, (2011), 295-304.
6. Gong, N., Wang, J. and Sridhar, R., "Variation aware sleep vector selection in dual ${\rm v} _ {{{\rm t}}} $ dynamic or circuits for low leakage register file design", ***IEEE Transactions on Circuits and Systems I: Regular Papers***, Vol. 61, No. 7, (2014), 1970-1983.
7. Peiravi, A. and Asyaei, M., "Current-comparison-based domino: New low-leakage high-speed domino circuit for wide fan-in gates", ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems***, Vol. 21, No. 5, (2013), 934-943.
8. Moradi, F., Cao, T.V., Vatajelu, E.I., Peiravi, A., Mahmoodi, H. and Wisland, D.T., "Domino logic designs for high-performance and leakage-tolerant applications", ***Integration, the VLSI Journal***, Vol. 46, No. 3, (2013), 247-254.
9. Asyaei, M., "A new leakage-tolerant domino circuit using voltage-comparison for wide fan-in gates in deep sub-micron technology", ***Integration, the VLSI Journal***, Vol. 51, (2015), 61-71.
10. Nasserian, M., Kafi-Kangi, M., Maymandi-Nejad, M. and Moradi, F., "A low-power fast tag comparator by modifying charging scheme of wide fan-in dynamic or gates", ***Integration, the VLSI Journal***, Vol. 52, (2016), 129-141.
11. Asyaei, M. and Ebrahimi, E., "Low power dynamic circuit for power efficient bit lines", ***AEU-International Journal of Electronics and Communications***, Vol. 83, (2018), 204-212.
12. Mahmoodi-Meimand, H. and Roy, K., "Diode-footed domino: A leakage-tolerant high fan-in dynamic circuit design style", ***IEEE Transactions on Circuits and Systems I: Regular Papers***, Vol. 51, No. 3, (2004), 495-503.
13. Alioto, M., Palumbo, G. and Pennisi, M., "Understanding the effect of process variations on the delay of static and domino logic", ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems***, Vol. 18, No. 5, (2010), 697-710.
14. Asyaei, M., "A new low-power dynamic circuit for wide fan-in gates", ***Integration, the VLSI Journal***, Vol. 60, No., (2018), 263-271.
15. Wang, J., Wu, W., Gong, N. and Hou, L., "Domino gate with modified voltage keeper", in Quality Electronic Design (ISQED), 2010 11th International Symposium on, IEEE. (2010), 443-446.

A New Circuit Scheme for Wide Dynamic Circuits

M. Asyaei

School of Engineering, Damghan University, Damghan, Iran

P A P E R I N F O

Paper history:
Received 06 November 2017
Received in revised form 07 December 2017
Accepted 16 Januray 2018

Keywords:
Dynamic circuit
Keeper
Leakage current
Noise immunity
Wide fan-in gates

A B S T R A C T

در این مقاله، یک طرح مداری جدید برای کاهش توان مصرفی مدارهای دینامیکی پیشنهاد می‌شود. در مدار پیشنهادی، از یک ترانزیستور نگهدارنده از نوع NMOS برای حفظ سطح ولتاژ گره خروجی در مقابل تسهیم بار، جریان نشتی و منابع نویز استفاده شده است. با بکارگیری طرح نگهدارنده پیشنهادی، دامنه تغییرات ولتاژ گره دینامیکی کاهش داده می‌شود تا توان مصرفی گیت‌های عریض کم گردد. همچنین، با استفاده از ترانزیستور پایه در حالت دیودی، جریان نشتی زیرآستانه کم می‌شود و در نتیجه، مصونیت در برابر نویز مدار پیشنهادی افزایش می‌یابد. نتایج شبیه‌سازیهای گیت‌های OR عریض در فناوری ۹۰ نانومتر CMOS، ٤٨ درصد کاهش توان مصرفی و ١/٦٥ برابر بهبود مصونیت در برابر نویز را برای گیت‌های ٣٢OR بیتی در تاخیر یکسان در مقایسه با مدار دینامیکی متداول نشان می‌دهد.

***doi**: 10.5829/ije.2018.31.04a.03*