



## A Study on the Electrical Conductivity of Coated Fe-17%Cr Alloy Used in SOFCs

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### Abstract

Spinel coatings that contain cobalt are hopeful candidates for Solid oxide fuel cell (SOFC) interconnect applications because of their high conductivity. The purpose of this work was to investigate the electrical conductivity of AISI 430 stainless steel which was coated in a Co-base pack mixture by pack cementation method. Electrical conductivity of the coated substrates was tested as a function of temperature by annealing the samples from room temperature to 800 °C. Also electrical conductivity has been investigated as a function of oxidation time during isothermal oxidation at 800 °C. Results showed the increase of temperature caused to the decrease of electrical conductivity. Result of X-ray diffraction pattern exhibited, that the coating layer transformed to  $MnCo_2O_4$  and  $CoCr_2O_4$  spinels during annealing in isothermal oxidation. These spinels improved electrical conductivity of coated substrates ( $103 \text{ S.cm}^{-1}$ ) compared to uncoated substrates ( $27.7 \text{ S.cm}^{-1}$ ) after 200 h oxidation at 800 °C.

**Keywords:** Electrical conductivity, Solid oxide fuel cell (SOFC), AISI 430 ferritic stainless steel, Spinel

### 1. Introduction

Solid oxide fuel cell (SOFC) technology has become increasingly attractive as a power generation method because SOFC have lower emissions and higher efficiency relative to traditional energy-conversion systems. Interconnects are critical part of planar SOFC designs. The interconnect is needed to connect the individual cells in an SOFC stack electrically, and also separates air or oxygen on the cathode side from fuel on the anode side. Therefore, the requirements of interconnects are quite demanding, i.e., maintenance of high electrical

conductivity, good stability in both reducing and oxidizing atmospheres, and close CTE match with other SOFC ceramic component [1]. Doped lanthanum chromite has been widely used as SOFC interconnect when operating at high temperature (1000 °C). However, these chromite interconnects are relatively expensive (especially for planar type stacks) as well as being brittle and difficult to fabricate. The reduction in the operating

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temperature of SOFC from 1000 °C to 600–800 °C leads to the potential for using lower cost metallic interconnects materials such as stainless steel. Relative to their ceramic counterpart, metallic interconnects have improved stability, electrical conductivity, thermal conductivity, ease of manufacturing, and are less costly to manufacture [2]. Almost all of the candidate alloys being considered for this application are chromia forming alloys due to the acceptable electrical conductivity and stability of Cr<sub>2</sub>O<sub>3</sub>. However, as the scale for these alloys increases, scale electrical resistance also increases, and chromium evaporation can lead to cathode poisoning, and thus shorten the required service life for the SOFC stack. In order to solve the mentioned problems, spinel coatings can be employed. Numerous techniques have been developed to apply coatings to ferritic stainless steels. These include slurry coatings [3-6], anodic electrodeposition [7], cathodic electrodeposition of particular metals or alloys, followed by annealing/oxidation in air and pack cementation [8-11]. The latter method has been attracting attention due to its low cost, ease of fabrication, good adhesion between the deposited coating and substrate and extensive application.

The objective of the current work was to evaluate the electrical conductivity of coated AISI 430 specimens which were coated in a Co-base pack mixture by pack cementation technique.

## 2. Experimental procedure

Samples of AISI 430 stainless steel, measuring 10 mm × 5 mm × 2 mm with chemical composition of 17.4% Cr, 0.92% Mn, 0.85% Si, 0.12% C, 0.02% S, 0.03% P with Fe as remaining were used as substrates. Specimens were polished from 320-grit sic paper up to 1200-grit, ultrasonically cleaned in ethanol and dried. In order to deposit cobalt onto the substrate, pack cementation method was employed. Co, Al<sub>2</sub>O<sub>3</sub> and NH<sub>4</sub>Cl powder were used as powder mixture in average size of 1 μm, 70-80 μm and 240 μm. The optimized conditions for coating of cobalt onto the surface of AISI 430 stainless steel by pack cementation in the previous work [12] were identified: 10% wt. Co, 1% wt. NH<sub>4</sub>Cl, 89% wt. Al<sub>2</sub>O<sub>3</sub> as powder mixture and annealing at 800 °C for 3 h at presence of Ar gas. After pack cementation treatment, the samples were removed from the pack and ultrasonically cleaned in ethanol to remove any embedded pack material.

Electrical conductivity measurement of the oxidized samples was accomplished by employing the set-up shown in Figure 1. Platinum wires were spot welded to one side of two identical polished samples to provide electrical connections. To avoid alloy-to-alloy adhesion and erroneous results, platinum wire welded specimens were pre-oxidized for 24 h at 800 °C. No conductive paste, which may affect the oxidation mechanism, was applied between the two samples. A constant current density of 500 mA cm<sup>-2</sup> was applied and the voltage was recorded every 30 minutes. An ammeter and a voltmeter were employed for this purpose. The data were used to calculate the conductivity according to Ohm's law and the electrical conductivity as a product of the conductivity and surface area. In order to measure the resistance contribution from the junctions, wires and the alloy, two platinum wires were spot welded to the sides of a single AISI 430 specimen and the resulting resistance was subtracted from the original test results. Electrical conductivity was measured as a function of different temperatures (400-800 °C) for 200 h and as a function of time at 800 °C. The above-mentioned tests, were run at an electric box furnace and static air.



Cross-section microstructure and chemical composition of coated specimens were analyzed using scanning electron microscopy (SEM) (Camscan MV2300) with energy dispersive spectroscopy (EDS). X-Ray diffraction (XRD) was used to identify phases formed in the surface layer of as-coated and oxidized specimens with a Philips X'Pert High Score diffractometer using Cu K $\alpha$  ( $\lambda = 1.5405 \text{ \AA}$ ).

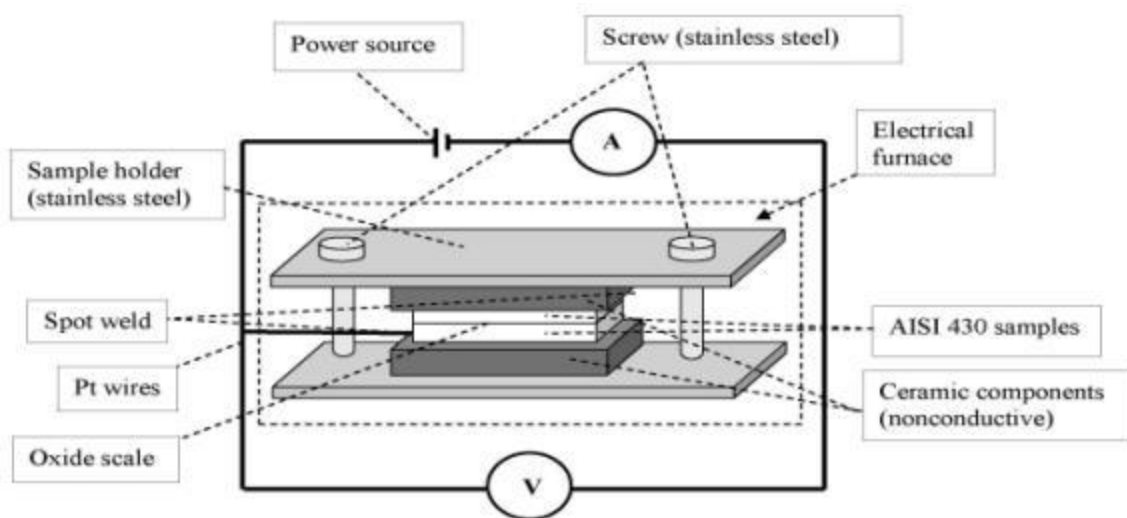


Figure. 1. Experimental set-up for measuring the electrical contact resistance of oxide scales.

### 3. Results and discussion

#### 3.1. Coating of substrate

Figure 2 shows cross-sectional SEM image (Figure 2a) and EDS line scan (Figure 2b) of a coated sample. The deposited layer has good adherence to the substrate with no void, pore and discontinuity. Figure.2 shows an XRD diffraction pattern of a coated specimen. The identified phases include, CoCr and MnCo<sub>2</sub>O<sub>4</sub>. There are Ferrite and FeCr peaks from the substrate surface that overlap with the MnCo<sub>2</sub>O<sub>4</sub> and CoCr peaks. MnCo<sub>2</sub>O<sub>4</sub> spinel has acceptable electrical conductivity that can reduce the Area-specific resistance (ASR), which is required in interconnects.

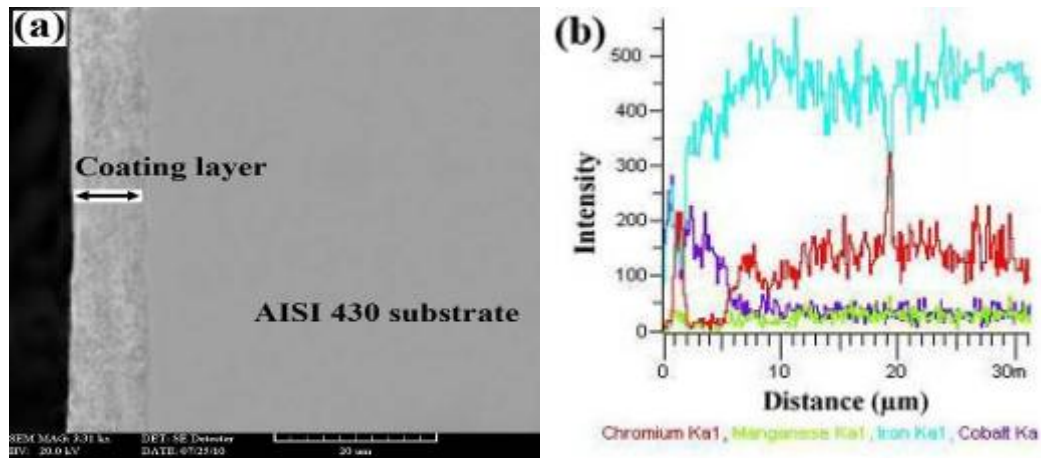


Figure 2. SEM cross section image of coating (a) and EDS line scan (b)

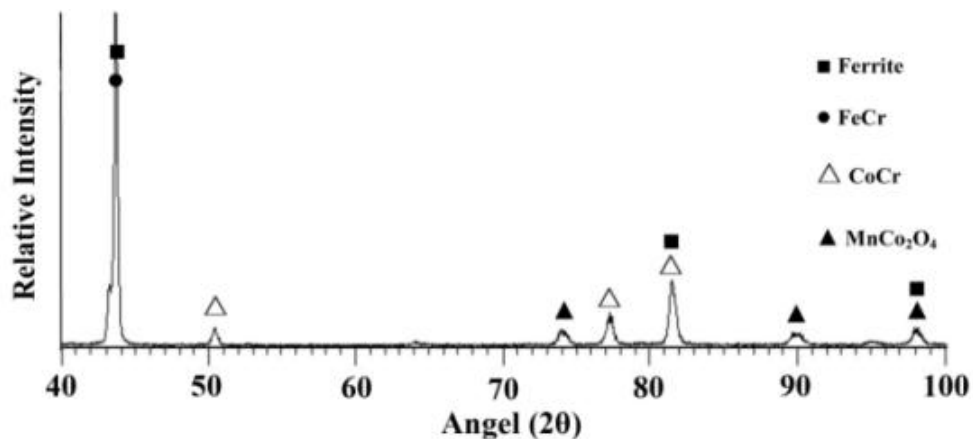


Figure 3. XRD pattern of coated specimen.

### 3.2. Evaluation of electrical conductivity

#### 3.2.1. Evaluation of electrical conductivity as a function of temperature

In order to investigate the influence of temperature on the Electrical conductivity, the electrical conductivity was measured at different temperatures (from room temperature to 800 °C) for uncoated and coated samples after pre-heating at 800 °C for 24 h. Figure. 4 illustrates the electrical conductivity as a function of temperature. By increasing the temperature the electrical conductivity decreases. This reasoning can be proved by the following equation [13]. The electrical conductivity of an oxidized alloy can be expressed as

$$\frac{1}{\sigma} = \frac{T}{\sigma^* \exp(-E_c/kT)} = \frac{T}{\sigma^*} \exp\left(\frac{E_c}{kT}\right) \quad (1)$$



where  $\sigma$  is electrical conductivity,  $\sigma^*$  is pre-exponent constants,  $E_c$  is the activation energy barrier for the conduction process,  $k$  is Boltzmann constant, and  $T$  is temperature. Based on this equation, the increase of temperature redounds to the decrease of electrical conductivity. Also at higher temperatures the more thickness of coating layer or substrate is affected by the oxidation reactions and therefore the thickness of chromia will increase and based on the Eq. (1) the electrical conductivity will decrease. In all temperatures the electrical conductivity of coated specimens was higher than the uncoated ones. This is because of the chromia scale that is created on the bare substrate during annealing. The chromia conductivity is considerably lower than the coated substrate which was covered with coating layer and it caused to the lower values of electrical conductivity [14].

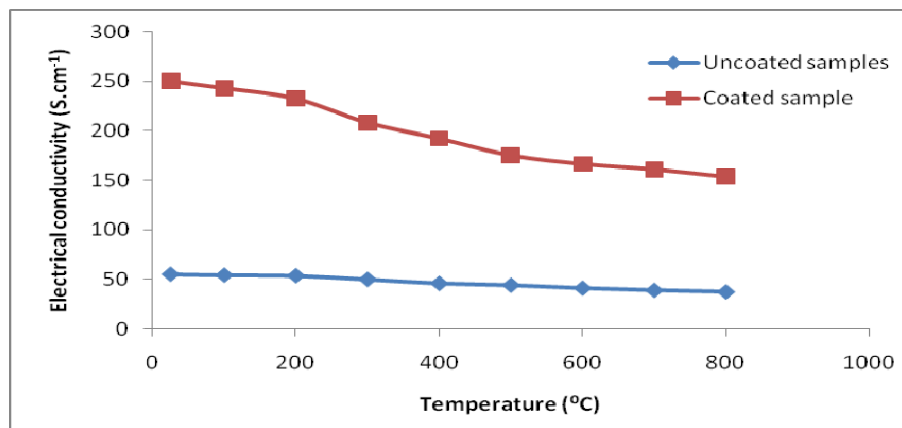


Figure. 4. Electrical conductivity values as a function of temperature for uncoated and coated

### 3.2.2. Evaluation of electrical conductivity as a function of time

The electrical conductivity for coated and uncoated AISI 430 stainless steel, as a function of time were plotted in Figure 5. Electrical conductivity values for uncoated substrates decrease with oxidation time and approach a value of  $27.7 \text{ S.cm}^{-1}$  after 200 h isothermal oxidation. Coated specimens however, exhibited a very low resistance ( $103 \text{ S.cm}^{-1}$ ) after 200 h. Figure. 6 shows XRD pattern of uncoated (Figure. 6a) and coated (Figure. 6b) specimens after 200 h isothermal oxidation. In XRD pattern of bare substrate  $(\text{Mn,Cr})_3\text{O}_4$  spinel, chromia and silica are observed. Presence of  $(\text{Mn,Cr})_3\text{O}_4$  spinel on the surface of bare substrate refers to ferritic stainless steels that normally containing small levels of Mn. When the alloy is subjected to the temperature range of  $650 - 850 \text{ }^\circ\text{C}$  the  $(\text{Mn,Cr})_3\text{O}_4$  spinel layer will be formed which is non-protective [15]. Also the chromia which is protective will be formed under the  $(\text{Mn,Cr})_3\text{O}_4$  spinel layer [15]. The electrical resistance of commercially available steel interconnects increases rapidly as the oxide scale grows [16].

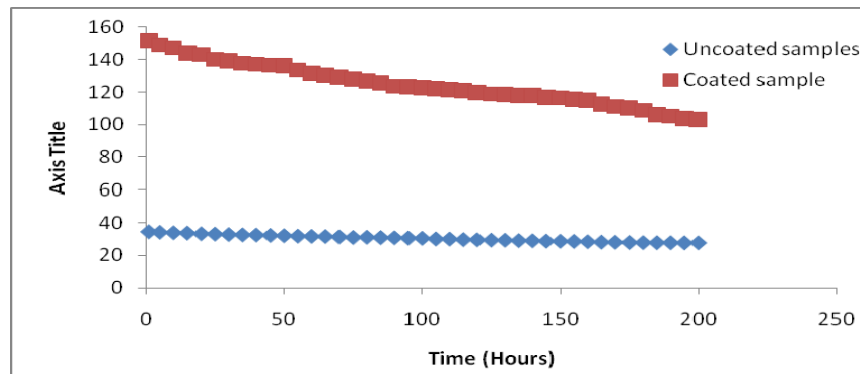


Figure 5. Electrical conductivity values as a function of time for uncoated and coated samples in isothermal oxidation.

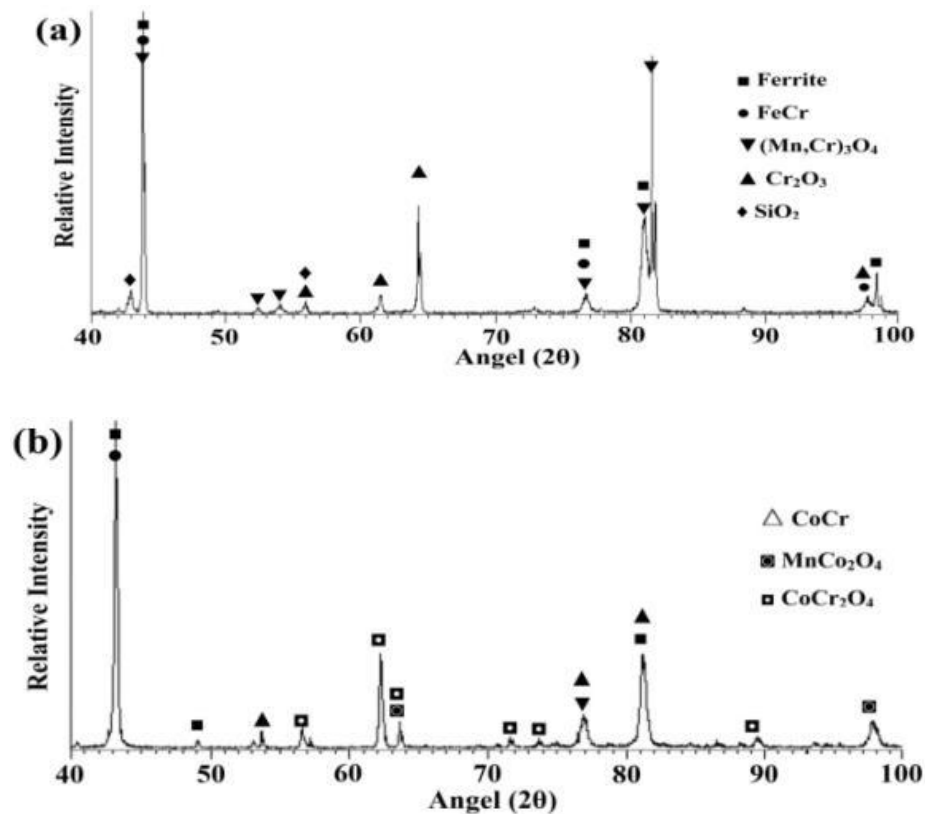


Figure 6. XRD pattern of (a) uncoated and (b) coated specimens after 200 h isothermal oxidation at 800 °C.

There are several factors can contribute to the increased resistance. The primary factor is the growth of the oxide scale [17]. The conductivities of both  $(\text{Mn,Cr})_3\text{O}_4$  spinel and chromia are considerably smaller in comparison with the metallic substrate [14]. An increase in the thickness of the oxide scale, therefore, proportionally decreases the electrical conductivity. The formation of an insulating silica layer as the result of interfacial segregation of Si is



another important factor which can negatively affects the electrical conductivity of steels containing Si. There are also other contributions to increased electrical resistance that are related to the metal/oxide scale interface. Interfacial imperfections, including voids and cavities as well as impurity segregation, reduce the scale-to-metal adhesion and actual surface area of intimate contact between the metal and oxide scale and, consequently, increase the interconnect electrical resistance [17].

The formation of  $\text{MnCo}_2\text{O}_4$  and  $\text{CoCr}_2\text{O}_4$  spinels during oxidation improved the electrical conductivity. Electrical conductivity of these spinels is remarkably higher than  $(\text{Mn,Cr})_3\text{O}_4$  spinel and chromia. Several factors can contribute to the improved electrical conductivity for the coated substrate over uncoated ones. These include the higher electrical conductivity of the scale consisting of spinels layer, the absence of silica phase, improved adhesion of oxide scale spallation and cracking. The spalled surface and the probable existence of cavities in the bare substrate reduce the actual contact surface area between the alloy and scale [18-20]. This caused to the lower electrical conductivity value, which is the product of resistance the nominal contact surface area of the scale and alloy.

#### 4. Conclusion

AISI 430 ferritic stainless steel was coated in a Co-base pack mixture. Electrical conductivity of coated and uncoated samples was investigated as a function of temperature and time. The formation of  $(\text{Mn,Cr})_3\text{O}_4$  spinel, chromia and silica during oxidation on the surface of AISI 430 caused to the lower values of electrical conductivity because of considerable higher electrical resistance of these compositions in comparison with the bare substrate. The application of spinel compositions ( $\text{MnCo}_2\text{O}_4$  and  $\text{CoCr}_2\text{O}_4$ ) increased the high temperature electrical conductivity of AISI 430 ferritic stainless steel used for SOFC interconnects. The electrical conductivity was obtained  $103 \text{ S.cm}^{-1}$  for coated samples and  $27.7 \text{ S.cm}^{-1}$  for uncoated samples after 200 h annealing in static air at  $800^\circ \text{C}$ .

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