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Evaluation and designing a fault detection system and tolerance in analog and digital circuits

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Abstract
Accurate fault detection in term of the parameters such as voltage, current, gain and overall consumed energy in digital and analog circuits needs circuit simulating using accurate parameters under the real condition and real inputs. The reason for needing the fault correction operation in the destination is reduction of the transmission fault and lack of requiring the transmitters' power increase. Of course, is should be noted that since the fault correction operation in required to add extra information to the transmitted data; the transmission rate would be higher which needs more bandwidth. Also, block codes, convolution coded and mix operation are described. Using the block coding which is performed on the bit's blocks, it is possible to reduce the fault in decoded data. Using the convolution encoding and hamming code which is applied on each of the bits, in addition to reducing the fault possibility in decoded data, it is possible to change the code rate considering the channel conditions such as raining etc. Making use of the mixing operation also causes the security of the transmitted information against fading, batching and etc. in this paper, by investigating the fault correction methods, we will investigate the low cost fault detection (LCFD) in all single-bit complex circuits and evaluate the characteristics of the circuit in vicinity of the fault.

Keywords : Fault detection system , Fault tolerance , analog and digital circuits, FEC,LCFD

Introduction

The fault detection and correction plans are systematic and unsystematic. In systematic plan, the transmitter transmits the main data with a fixed rate of numbers as bits in which the evaluation bits are obtained from a certain algorithm, which make use of the main data. If only the fault detection was considered, the receiver can compare the algorithm again on the run main data and its output value with evaluating bits. If the result was the same, there would not be any fault. In systems making use of the unsystematic code, the main message is converted to a code message. The suitable performance is achieved when they are selected based on the telecommunication channels characteristics and data transmission plans. The conventional types of the telecommunication channels include a model without memory in which the fault occurs randomly and with a certain probability and the model is dynamic.

Consequently, the fault correction and detection can be divided into random fault correction/detection and burst fault detection/correction. If the capacity of the channel cannot be determined or the capacity is over-changing, one can request re-transmission of data which is recognized as an automatic repeat request which is applicable particularly in internet. The fault correction and detection are in 2 ways:

Automatic repeat request: data are received in for a block each of which is investigated for the fault. If there was any fault, the request is for data block automatically to be repeated, this process continues so that the all data are received in correct form.

- **Forward fault correction**: the transmitter encodes the information using ECC before sending. The extra information is used for retrieving the main information by receiver.

These 2 methods may be combined and there would be another method called hybrid automatic repeat request.

Fault detection method

Controlling

Fault detection method in information is usually calculated by summing a set of values. Usually, the controlling sum for calculation of data and comparison is added to the end of data. For example, in xmodem which is protocol in file transmission, the controlling sum is calculated irrespective of its overflow. The controlling sum is not always able to detect all faults. This is used in BBS. In data 1 received the information identity is similar to the transmitted data, but in 2 the identity is different. This method cannot detect the fault since the controlling sum of the transmitted data is similar to the received one.

Destination fault detection

The technique is used in order to control the fault which includes the redundant bits and the receiver makes use of these redundant data in order to detect the fault (parity bit)

Parity bit

In communication, the simple for of the fault detection is used using a redundant bit after the data bits and before the stop bits. The parity bit has different types: even parity, odd parity, sign parity, distance parity. A frame of data using the parity bit is as follow.

Generally is a transmitting system, the transmitted information may be changed due to the noise or intervention. For this reason, in order to make sure of the achieving the correct information in receiver, the fault correction and detection methods are used. The level of EDC required and its effectiveness in correct information retrieve depends on the SNR.

Transmitted signal power enhancement

This method is similar to that in a noisy room, we speak louder. Therefore, the SNR increases and leads to the reduction of the received fault. Assuming that the signal transmission environment features are not changeable, the most evident method is the transmitters' power increase which is not always possible. The reason for this issue is that majority of the telecommunication equipment are designed so that they can work to their maximum power. Of course, if it was possible to increase the transmitter's power, there would be major problem which is the fact that the strengtheners' characteristics are not linear and power increase means the main signal strengthening as well as noise strengthening which worsens the conditions.

Signal noise reduction

In order to understand this method, assume that you are in a crowded room. Consequently, in order to be able to speak easily you go to a corner of the room which has less noise which means the noise reduction. In telecommunication equipment only some types of the noise are controllable including thermal and inter-modulation noises. So, assuming that telecommunication systems design is such that these 2 noises are minimum; there would be no other method for noise reduction.

Diversity

When you are listening to radio and feel that the signals are constantly increasing and reducing, your reaction is that you change the location of the radio (it is similar to the mobile phones). In satellite telecommunication, in rainy zones, usually there are 2 terrestrial stations in certain distance both of which receive a signal in order to increase the SNR. Different polarizations, which are used to develop the useful spectrum in satellite telecommunication, can be used for similar information which is a fault correction method. All mentioned methods are as diversities whose main goal is to increase the signal quality with increasing the telecommunication stations.

Automatic repeat request (ARQ)

In this method, the transmitter buffers the transmitted information until the correct information recovery message is received. As the correct information recovery message is received, the transmitted information are removed from the memory and in case of receiving ARQ, the mentioned information would be transmitted again. It is necessary to note that this method needs two-wire transmission.

FEC

When it is not possible for two-wire transmission, the FEC is used for fault correction using which the fault rate decreases. In this method, there is no need to increase the transmitters' power and only by adding the extra information to the main transmitted one, it is possible to retrieve the transmitted information. Of course, it should be noted that adding information to the main data means higher transmission rate which needs more bandwidth. But, anyway, using this method the transmission system would be simple and the operational load of the fault detection and correction is on the receiver which means the decrease of transmitter's complexity. The fault detection and correction operation in digital telecommunication systems which is introduced as channel coding would be explained in the following in order to cope with factors such as thermal noise, burst noise (group unwanted signals which deteriorate a part of data), channel fading etc.

There are 2 principal techniques in order to correct the faults"

First one is called retransmission. In this method, the receiver, using redundant and controlling bits, detects the fault in message and send a message to the transmitter and request for retransmission.

The second method is forward fault detection. In this method, not only it is discovered the message us faulty, but using the redundant bits and particular techniques also it is attempted to guess the mentioned message.

Error detection methods

1. **Controlling sum method**

Fault detection method in information is usually calculated by summing a set of values. Usually, the controlling sum for calculation of data and comparison is added to the end of data. For example, in xmodem which is protocol in file transmission, the controlling sum is calculated irrespective of its overflow. The controlling sum is not always able to detect all faults. This is used in BBS. In data 1 received the information identity is similar to the transmitted data, but in 2 the identity is different. This method cannot detect the fault since the controlling sum of the transmitted data is similar to the received one.

2. **Destination fault detection**

The technique is used in order to control the fault which includes the redundant bits and the receiver makes use of these redundant data in order to detect the fault (parity bit)

Proposed circuit design

In this section, we design the complex circuit and investigate it:

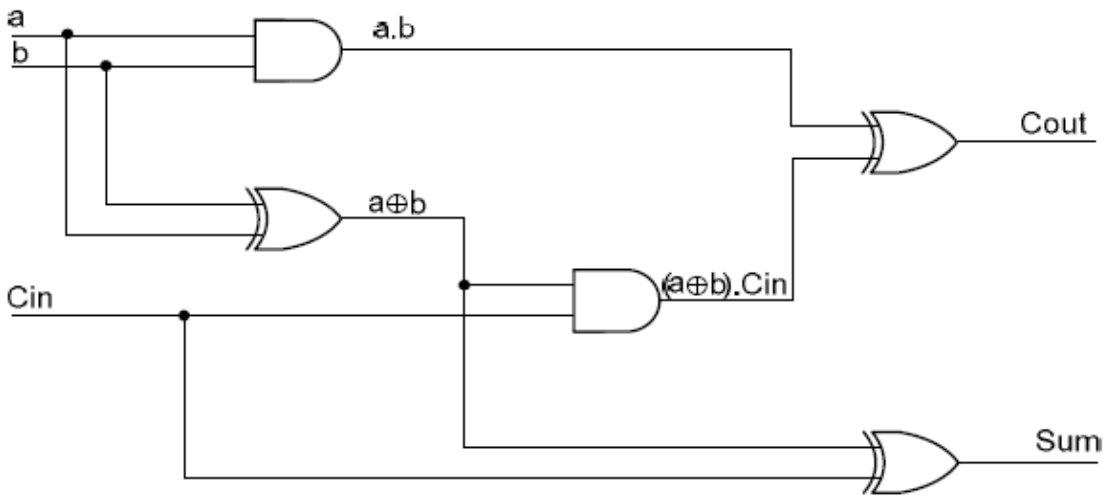
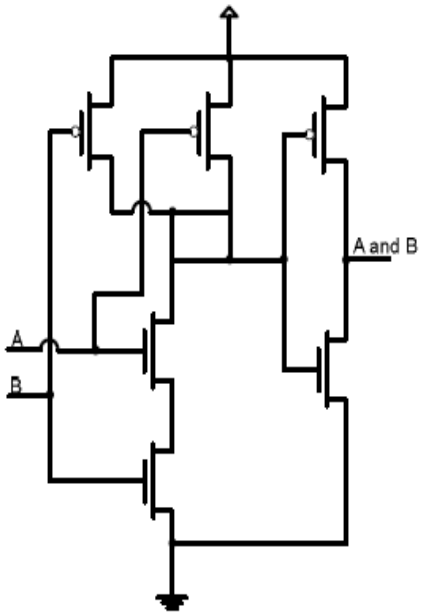


Fig1. Collector complex circuit

SP1	SP2	SP3	SP4	SP5	SP6	SP7	SP8
a	b	Cin	a and b	a xor b	(a xor b) and Cin	Sum	Cout
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	1	0	1	0
0	1	1	0	1	1	0	1
1	0	0	0	1	0	1	0
1	0	1	0	1	1	0	1
1	1	0	1	0	0	0	1
1	1	1	1	0	0	1	1

Fig2. The results table of the collector complex circuit

The simulation and error detection is performed using LCFD considering which, we have:



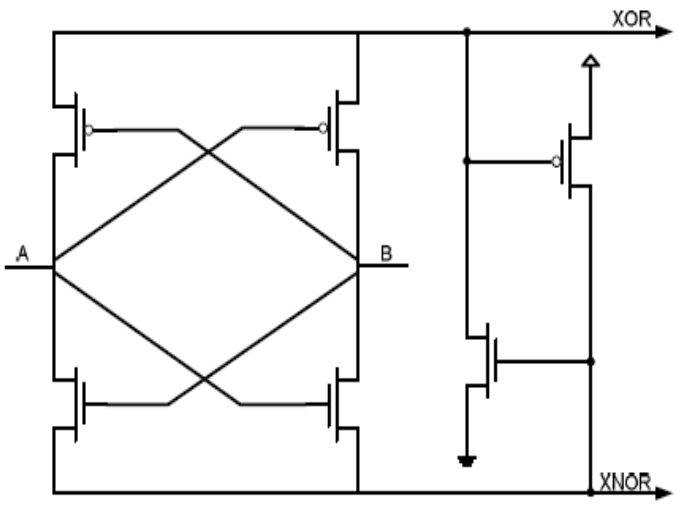


Fig3. Left) collector with complementing AND, right) with XOR gate

The parity checker circuit for this idea is designed as follow:

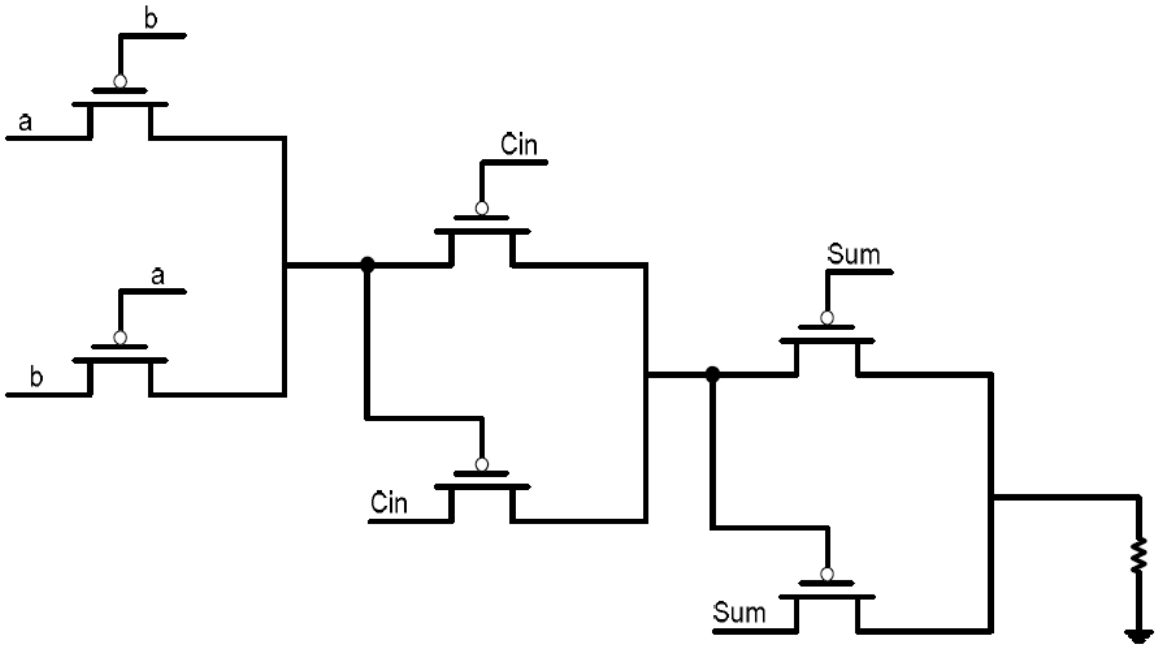


Fig4. Parity checker circuit

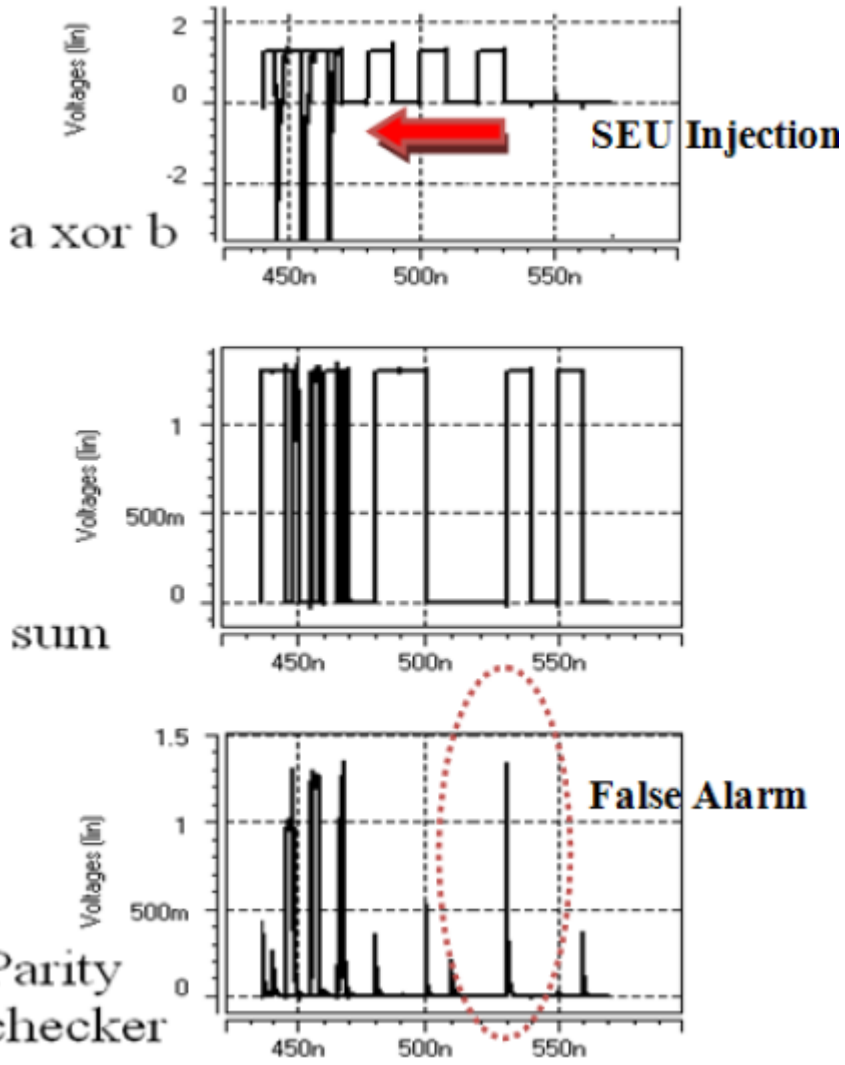


Fig5. The changes in output by fault injection

Tech Size[nm]	130
Average Power[µW]	5.756
%Power Overhead	24.5
Max Delay[ns]	0.244
Power-Delay Product[aJ]	1.404

Fig6. Output features table in 130 nm technology

Conclusion

In this article, different types of the error detection method were evaluated and by AND an XOE circuits we could design a collector which is able to detect the errors and faults. Every new circuit, in addition to the fact that can perform to the necessary extent and improve a part of the performance, can deteriorate the operation in other section. In other word, always there are giving and takings in in designing the analog and digital circuits design. Here, in addition to the fact we could improve the circuit's ability applying the fault detection, the occupied area of the circuit increased which, as a result, our consumption power also increases which is a defects in designing in electronic world.

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