2nd INTERNATIONAL CONFERENCE ON
RESEARCH IN SCIENCE AND TECHNOLOGY
Istanbul-Turkey 14 March 2016
RSTCONF
دومین کنفرانس بین المللی
پژوهش در علوم و تکنولوژی
ترکیه - استانبول ۲۴ اسفند ۱۳۹۴

Comparative Study of Trigate SOI FinFET and Trigate JL SOI FinFET Structures

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Abstract
This paper investigates the effect of channel length variations on transistor perfomane for the Trigate SOI FinFET and Trigate Junctionless SOI FinFET. compaires the variations in threshold voltage, transeconductance , subthreshold swing, I_{ON}/I_{OFF} ratio and r_o.

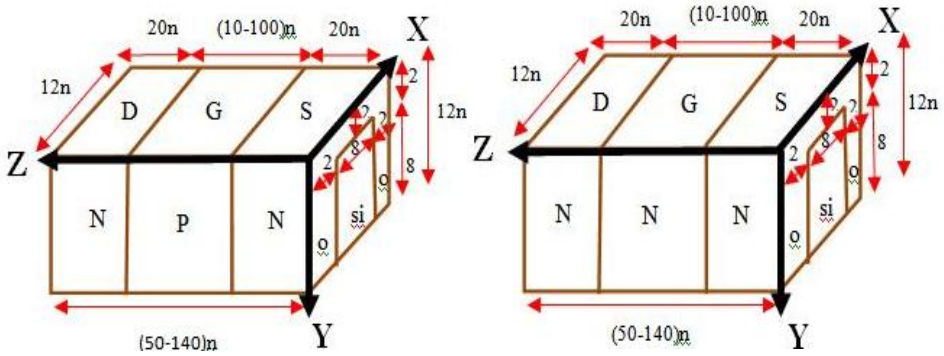
Keywords: FinFET, Junctionless, SOI, SCEs, V_{th} , subthreashold slop, I_{ON}/I_{OFF}.

Introduction

As the gate length decreases the gate control over the channel also decrease due to the proximity of source and drain. The gate can be placed close to the channel by taking ultra thin body known as fin type structure and tighter gate coupling can be achieved by increasing the number of gates from single gate to multi gates. The multi gate FinFET transistors are very promising alternatives to planar devices in sub 50nm gate length regime. The tri gate FinFET [1] is one of the promising structures in nano scale regime. The tri gate FinFET provides a symmetric device architecture where the channel is controlled by gate from three sides of the Si film. The FinFET can be fabricated on either bulk silicon (bulk-Si) or silicon-on-insulator wafer substrates [2],[3]. FinFETs have advantages like a higher I_{ON}/I_{OFF} ratio (very important for digital circuits) and smaller intrinsic gate capacitances and design flexibility at with multiple gates [4]. The junctionless transistor is considered as one of the most promising candidates for nanometer scale CMOS integrated circuits [5]. The concept of the junctionless(JL) nanowire transistor(JNT), which contains a single-doping species at the same level in its source, drain, and channel, has been investigated[6-13]. The advantages of JL devices include: 1) avoidance of the use of an ultra shallow source/drain junction, which greatly simplifies the process flow; 2) low thermal budgets owing to implant activation anneal after gate stack formation is eliminated; and 3) the current transport being in the bulk of the semiconductor, which reduces the impact of imperfect semiconductor/insulator interfaces. However, the JNT devices require a silicon-on insulator (SOI) wafer and a uniform ultra thin channel to turn the device off, making them technologically difficult and expensive to produce. In this paper Trigate SOI FinFET and Trigate Junctionless SOI FinFET have been compared using extensive device simulations and investigated in the sence of electrical characteristics.

DEVICE STRUCTRURE AND SPECIFICATION

The transistor structures are illustrated in Fig. 1.



(a)Trigate SOI **(b)Trigate SOI**

Fig.1. Three dimensional view of FinFET's

The transistors under investigate have following specifications: physical models are performed for the following n-channel FinFET designs: physical gate length L_G=(10-100)nm, gate oxide thickness t_{OX}=2nm and supply voltage VDD=1V, channel doping N-type=1e19 and P-type=1e17. n-channel Junctionless FinFET has physical gate length L_G=(10-100)nm, gate oxide thickness t_{OX}=2nm and

supply voltage VDD=1V. channel doping N-type=1e19. The device parameters for Trigate SOI FinFET and Trigate Junctionless SOI FinFET have been sumerized in Table1.

Table1. Device

Device parameter	Trigate SOI FinFET	Tri-gate Junctionless SOI FinFET
Channel Length (nm)	10-100	10-100
t_{ox}(nm)	2	2
Gate work function(eV)	4.30	4.30
Channel Doping	N=1e19 P=1e1^{V}	1e19 (n-type)

Electrical characteristics for the devices are simulated using 3D device simulator ATLAS Version 3.20.2.R[14]. The gate and the drain voltages are swept from -1 to +1 V and 0 to 1V respectively. The physical gate length is changed between 10 to 100 nm. The transfer and the output characteristics, threshold voltage, subthreshold slope and drain induced barrier lowering (DIBL), g_m, I_{on}/I_{off} ratio, r_o are studied.

RESULTS AND DISCUSSION

The I_D-V_G characteristics of transistors are shown in Fig.2.

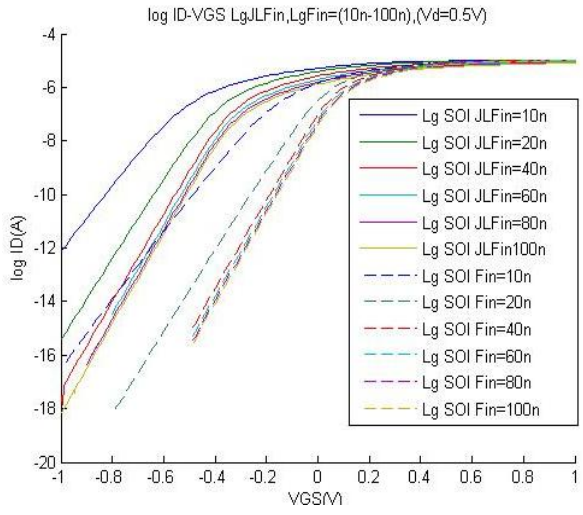


Fig 2. Simulated Trigate SOI FinFET and Trigate Junctionless SOI FinFET transfer characteristic (I_D-V_G)

Simulation results show that both Trigate SOI FinFET and Trigate Junctionless SOI FinFET have low leakage current. The I_D-V_D characteristics of the transistors are shown in Fig.3. Simulation results show that Trigate SOI FinFET has better output characteristic and higher ON currents when the channel length gets smaller.

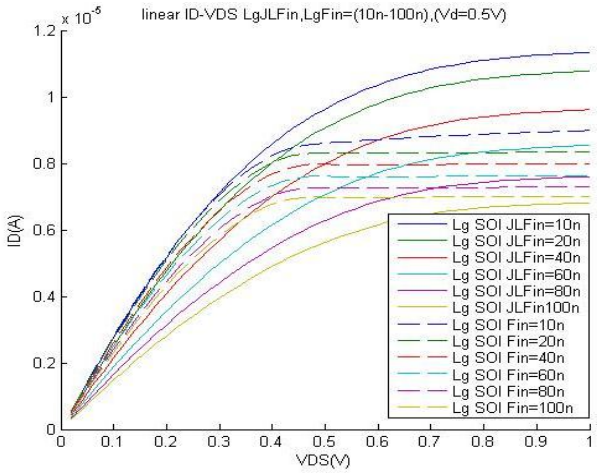


Fig.3. Simulated Trigate SOI FinFET and Trigate Junctionless SOI FinFET output characteristic (I_D-V_D)

A.Variation in Threshold Voltage (V_{th})

The change in threshold voltage with the channel length is shown in Fig.4. Although the threshold voltage of a MOSFET is not a figure of merit for device/circuit performance, it is the most important parameter for MOS device modelling and circuit design [15-17]. The result shows that threshold voltage is lower when channel length is scaled down therefore making it a good choice at smaller channel lengths.

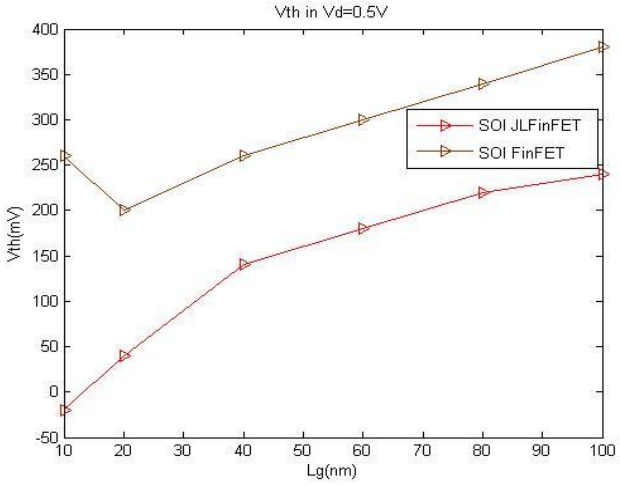


Fig.4. V_{th} versus to L_g variation

B. g_m

Fig. 5. shows g_m characteristics verses different channel lengths. G_m of the Trigate SOI FinFET is higher than that of the Trigate Junctionless SOI FinFET. This shows that FinFET exhibits higher voltage gain in analoge applications.

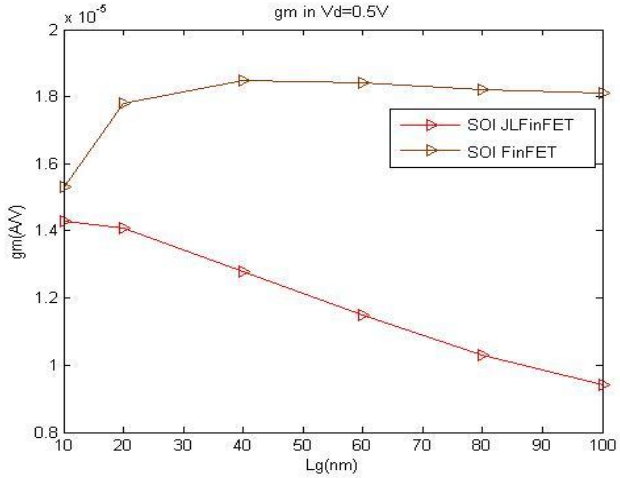


Fig. 5. g_m versus to L_g variation

C. Variation in subthreshold swing (SS)

Subthreshold swing is defined as the voltage change required to increase the drain current one order of magnitude[18]. Sub-threshold swing is a very critical parameter for a transistor[19]. Theoretical limit of sub-threshold swing of a MOSFET is 60 mV/decade[20]. Fig.6. shows the change in subthreshold swing with respect to channel length. Trigate SOI FinFET shows better subthreshold swing compared to Trigate Junctionless SOI FinFET at gate lengths below 60nm.

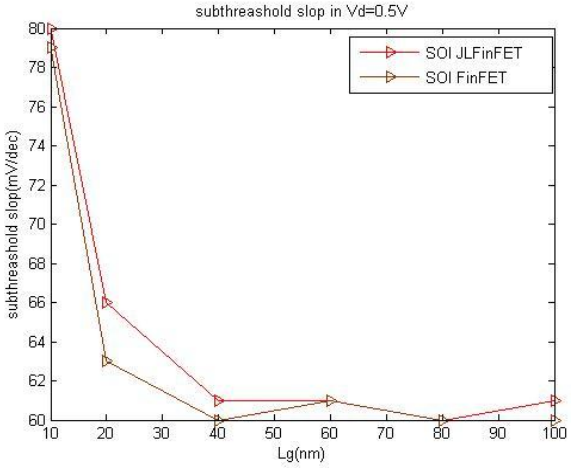


Fig.6. SS versus to L_g variation

D. I_{on}/I_{off} ratio

I_{on}/I_{off} ratios are critically affected when channel length comes down to the scale of 20 nm[20]. Fig.7. shows I_{on}/I_{off} ratio verses channel length. There is no much difference I_{on}/I_{off} ratio between Trigate SOI FinFET and Trigate Junctionless SOI FinFET. I_{on}/I_{off} ratio is better in some channel lengths for Trigate SOI FinFET and in other channel lengths for Trigate Junctionless SOI FinFET.

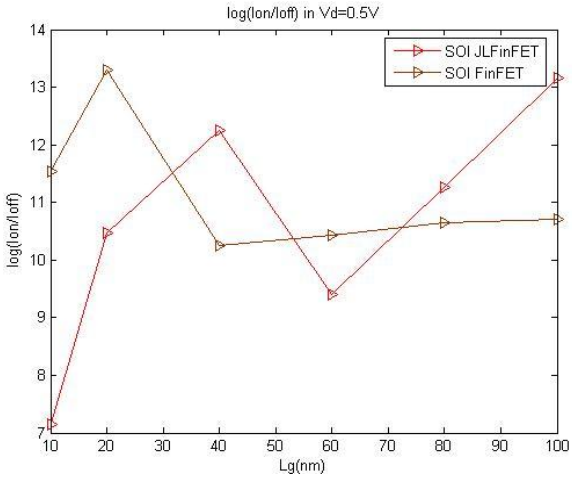


Fig.7. I_{on}/I_{off} ratio versus to L_g variation

E. r_O

Fig.8. shows the output resistance characteristics verses different channel length. The r_O of the Trigate SOI FinFET is higher than that of the Trigate Junctionless SOI FinFET. Higher output resistance along with high trancecondctance reveals that FinFET has higher gain which is very important in analoge and digital applications.

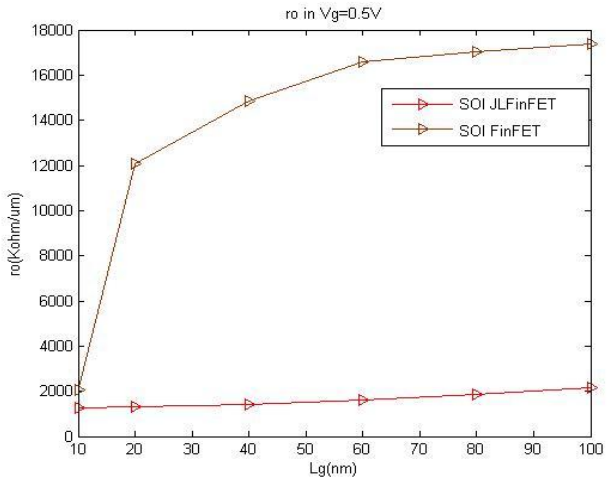


Fig.8. r_o versus to L_g variation

CONCLUSIONS

In this work, the short channel effects of Trigate SOI FinFET and Trigate Junctionless SOI FinFET for different channel lengths has been analyzed through device simulations. Results show that Trigate SOI FinFET have higher V_{th}, g_m, r_o and lower subthreshold slop in the scaled channel lengths. This means that FinFET with source and drain junctions to channel has better performance compaired to junctionless counterpart.

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