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Output Impedance Improvement of A Low Voltage Low Power Current Mirror Based on Bulk Driven Technique

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Abstract

This paper improved the output impedance of an LVLP current mirror by using bulk driven technique and transconductance enhancement. The applied technique increases the output impedance of current mirror significantly compared with the primary circuit. Also, it provide little improvement in input resistance and bandwidth. Operation principle of current mirror circuit with proposed improvement is discussed, the most important formulas are derived and compared with the primary circuit and its performance is verified by simulation in 0.18um technology. An output resistance of 39.5 GΩ is achieved for the improved circuit that shows 5GΩ increment in comparison with primary circuit. Besides, simulation results show an input resistance of 12.8 Ω and -3dB cut-off frequency of 216 MHz for the improved current mirror circuit while it consumes only 42.5 µW still and other specifications are still remain unchanged. Simulation is done by 1V power supply and 15µA input current.

Keywords: Low Power Current Mirror; Bulk Driven technique; High output Impedance; CMOS

Introduction

Current mirrors are one of the most important and efficient block of each analogue integrated circuit due to providing bias conditions and active loading role, thus optimum design has significant influence on circuit performances enhancement. Accuracy, linearity, output and input impedance, bandwidth and noise are the factors of the current mirrors which should be considered for optimum design (Azhari et al, 2011). On the other hand, in recent years low voltage and low power circuit designs are a substantial point according to frontier of knowledge in integrated circuit designs (Yani et al,2010).

High output impedance is one of the most important factor of each current mirror that many methods are proposed to achieve it. Cascode structure is a traditional method that supports this idea (Gabbouj et al, 2008), (Zhu et al, 2008). In some cases, QFGMOS transistors are used to increase output impedance (Raj et al, 2014). In some papers, presented a feedback gain stage to enhance this factor (Hsing et al, 2001). Also, in some cases, the features of the feedback structures such as shunt type is used to increase the output impedance (Sharma et al, 2006). Figure 1 shows another structure that not only does it increases output impedance but also enhance accuracy by equalization of drain-source voltage and decreasing channel length modulation. However, Conventional cascode current mirrors need more power supply. Thus due to importance of low voltage low power technology, some methods are considered to minimize voltage and power. For instance, using FGMOS transistors (Sharma et al, 2006) or bulk driven technique are suggested (Murphy et al, 2005).

Besides all benefits, some drawbacks are reported for these methods. For example, current offset problem and low bandwidth are reported as a consequence of using bulk driven technique (Azhari et al, 2011). So, achieving advantages of this idea needs wise and accurate circuit design to have an LVLP current mirror with bulk driven structure. Also, minimizing transistors width and length is another way to decrease power supply but nowadays, it has been limited by technology (Yani et al, 2010).

This paper improve the performance and the output impedance of an LVLP current mirror by using bulk driven technique. In section 2 and 3 the main concepts of idea are described and circuit analysis of current mirror is presented in section 4. Simulation results are presented in Section 5. Finally, the paper is concluded in Section 6.

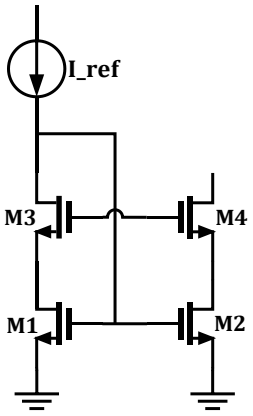


Fig 1. Cascode current mirror with high output impedance

Bulk driven and g_m boosting

Almost, depending on the applied technology the bulk of MOSFET transistor is connected to source terminal or power supply, V_{dd} (or V_{ss}) (Haga et al, 2005), in integrated circuit designs. But in some applications, this terminal can be used in another ways. Sometimes the bulk terminal connects to a dc bias voltage and will effect on bias conditions, which is known as body bias technique (Volta, 1832). Body driven technique modifies the effective g_m of MOSFET that it can change the circuit parameters. Fig. 2 illustrates the small signal model of a MOSFET with body effect.

According to nature rules of each transistor, following equations show g_{mb} calculation (Razavi, 2007):

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right) \quad (1)$$

$$\frac{\partial V_{TH}}{\partial V_{BS}} = -\frac{\partial V_{TH}}{\partial V_{SB}} = -\frac{\gamma}{2}\left(2\varphi_F + V_{SB}\right)^{-\frac{1}{2}} \quad (2)$$

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\varphi_F + V_{SB}}} = \acute{\eta} g_m \quad (3)$$

The first time, Balock et al. used bulk driven method for MOSFET analogue circuit design (Rajput and Jamuar, 2002). The aim of this work (Rajput and Jamuar, 2002) was any signal processing it is required some drain bias current to do. Gate driven circuits prepare this current when the gate voltage exceeds MOS threshold voltage, but in bulk driven circuits that is shown in Fig. 3, input signal is applied to bulk terminal and transistor is set in saturation region to make constant drain current.

This technique is useful in low voltage application. In the general case, bulk terminal is used in one of the three forms as follow. In first form that is shown in Fig. 4 (a), input signal is applied to gate terminal while bulk terminal effects on bias point through V_{bias} (Haga et al, 2005). Next form situation is vice versa, input signal is applied to bulk and bias voltage is connected to gate (Fig. 4 (b)) (Sharma et al, 2006). The final form which is the base of this paper idea, two input signals are applied, one of them is applied to gate and another one is applied to bulk terminal. Fig. 4 (c) shows this form clearly (Ebrahimi et al, 2015).

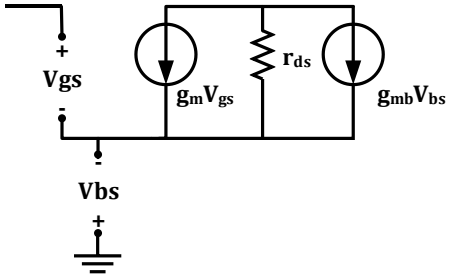


Fig 2. Small signal model of MOSFET with bulk terminal.

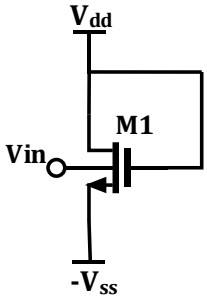


Fig 3. Bulk driven technique

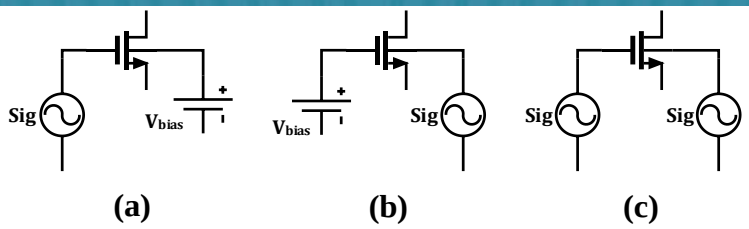


Fig 4. Body and gate derive techniques.

This technique also is used in differential pairs for some important applications (Rajput and Jamuar, 2002). One of the disadvantage of this idea is linearity problem in current mirror circuits, because the last transistor sets in saturation region thus input and output current do not have linearity, unlike in the gate driven current mirror. There are some suggestions to solve this problem according to applications (Yani et al, 2010).

Styling Current mirror performance enhancement by body driven technique

This paper presents an LVLP current mirror with high output impedance by applying the body driven technique to the current mirror circuit is proposed in (Azhari et al, 2011) that Fig. 5 shows the circuit diagram. Negative and positive feedbacks, the basic concept of the circuit, result in parameters improvement, such as high output impedance, low input impedance, desired BW, accuracy and low current transfer error.

The proposed idea is applying an extra signal to bulk terminal of M5 which is shown in Fig. 5. This new signal path that is shown with dash-line in Fig. 6, enhances the output impedance and improves the current transfer error of LVLP current mirror through effective gm boosting. It is worth mentioning that not only does the proposed idea have no bad effect on the other parameters, but also it improves them slightly.

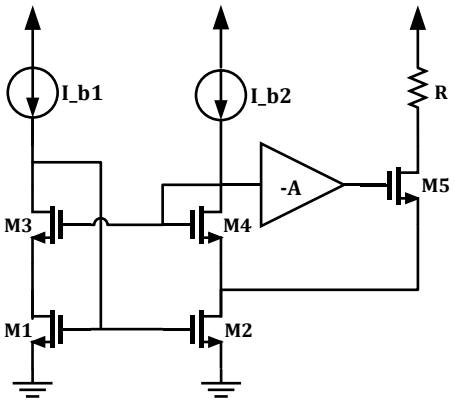


Fig 5. Current mirror circuit proposed in [1]

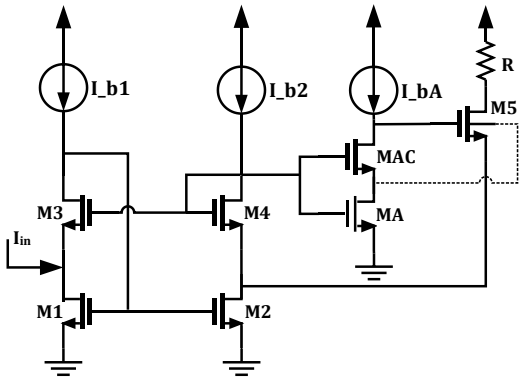


Fig 6. Schematic of current mirror with proposed idea.

PROPOSED CIRCUIT ANALYSIS

A. *Principle of operation*

The proposed circuit of this paper is based on circuit is shown in Fig. 5 which includes cascode current mirror comprised of four transistors M1-M4 that M4 is diode connected to have high output swing (Azhari et al, 2011). The output signal from drain of M4 transferred to M5 through gain boosting part (MA and MAC). From Fig. 6, it is obvious that there is another signal from drain of MA to bulk terminal of M5. Indeed, M5 has 2 amplified signal as input, one from MAC drain and another from MA drain. As mentioned in part 2, this technique increases the effective transconductance with g_{mb} factor which could change some parameters of whole circuit. The major change belongs to output impedance and also other parameter have little improvement. Analysis and mathematical calculations are described in next subsection.

B. *Output impedance*

One of the most significant factors of each current mirror is its high output impedance and low input impedance (Ramirez et al, 2005) (Garimella et al, 2005) (Cong and Geiger, 2000) .Using the bulk driven technique in final stage transistor, M5, increases output impedance while other parameters do not modify expressively. According to the circuit shown in Fig. 6, the output impedance of the current mirror with applied technique is equal to:

$$V_{\text{out}} = V_{\text{ds}} + V_{\text{d2}}$$

$$V_{ds5} = (I_{out} - g_{m5}V_{gs5} - g_{mb5}V_{bs5})r_{o5}$$

$$V_{gs5} = -(1 + A)V_{d2}$$

$$A = g_{mA}\left(\frac{g_{m,AC}}{g_{ds,A}g_{ds,AC} + g_{ds,bA}g_{m,AC}} || r_{ob,A}\right)$$

$$V_{bs5} = V_{dmA} - V_{d2}$$

$$V_{d,mA} = -V_{d2} \times g_{mA} \times R_{o,mA}$$

That $R_{o,mA}$ is equal to:

$$R_{o,mA} = r_{ds,mA} || \frac{r_{obA} + r_{ds,mAC}}{1 + g_{m,AC}r_{ds,AC}}$$

Thus:

$$V_{bs5} = -V_{d2}(1 + g_{mA}R_{o,mA})$$

$$V_{ds5} = r_{o5}I_{out} + g_{m5}r_{o5}(1+A)V_{d2} + g_{mb5}V_{d2}(1+g_{mA}R_{o,mA})$$

$$V_{d2} = (r_{ob2}||r_{o2})(I_{out} - g_{m2}V_{d3})$$

$$V_{d3} = -g_{m3}(r_{ob1}||g_{m3}r_{o3}r_{o1})(V_{d2} - V_{d1})$$

$$V_{d1} = -\frac{g_{m1}}{g_{m3}}V_{d3}$$

$$V_{d3} = -g_{m3}\,(r_{ob1}||g_{m3}r_{o3}r_{o1})(V_{d2} + \frac{g_{m1}}{g_{m3}}V_{d3})$$

$$V_{d3} = -\frac{g_{m3}(r_{ob1}||g_{m3}r_{o3}r_{o1})}{1+g_{m1}(r_{ob1}||g_{m3}r_{o3}r_{o1})}V_{d2}$$

$$V_{d2} = \frac{(r_{ob}||r_{o2})I_{out}}{1-\frac{g_{m2}g_{m3}(r_{ob2}||r_{o2})\,(r_{ob1}||g_{m3}r_{o3}r_{o1})}{1+g_{m1}(r_{ob1}||g_{m3}r_{o3}r_{o1})}}$$

$$V_{out} = I_{out}r_{o5} + V_{d2}\left[1+g_{m5}(1+A)r_{o5} + g_{mb5}r_{o5}\left(1+g_{mA}R_{o,mA}\right)\right]$$

$$R_{out} = r_{o5} + \frac{(r_{ob2}||r_{o2})}{1-\frac{g_{m2}g_{m3}R_2R_3}{1+g_{m1}R_3}}[1+g_{m5}(1+A)r_{o5} + g_{mb5}r_{o5}(1+g_{mA}R_{omA})] \quad (4)$$

Approximate calculation of the output impedance of the circuit shown in Fig. 5 is:

$$R_{out} = r_{o5} + \frac{(r_{ob2}||r_{o2})(g_{m5}(1+A)r_{o5})}{1-\frac{g_{m2}g_{m3}(r_{ob2}||r_{o2})}{1+g_{m1}}} \quad (5)$$

While the exact calculation of the output impedance of circuit shown in Fig. 5 is equal to:

$$R_{out} = r_{o5} + \frac{(r_{ob2}||r_{o2})}{1-\frac{g_{m2}g_{m3}R_2R_3}{1+g_{m1}R_3}}\left(1+g_{m5}(1+A)r_{o5}\right) \quad (6)$$

In all calculations, R2 and R3 are equal to:

$$R_2 = r_{ob2}||r_{o2} \quad (7)$$

$$R_3 = r_{ob1}||g_{m3}r_{o3}r_{o1} \quad (8)$$

Comparison of (6) and (4) shows that the applied bulk driven technique increases the output impedance of current mirror with following factor:

$$(r_{ob2}||r_{o2})/(1-\tfrac{g_{m2}g_{m3}R_2R_3}{1+g_{m1}R_3})[g_{mb5}r_{o5}(1+g_{mA}R_{omA})]$$

Also, comparison with other works shows that this idea has a very high output resistance for an LVLP current mirror.

C. Input impedance

It is good to have low input impedance for each current mirror. As mentioned, applied signal path to bulk of M5 does not significant effects on other parameters except output resistance and current transfer error. One of these parameters is input resistance that following steps show the input impedance calculation of proposed idea. Input resistance of Fig. 6 is equal to:

$$I_{in} = \left[\left(g_{m1} + \frac{g_{m3}g_{m1}}{(g_{m5}+g_{mb5})(1+A)}\right)\times K + G\right]V_{in} \quad (9)$$

Thus input resistor:

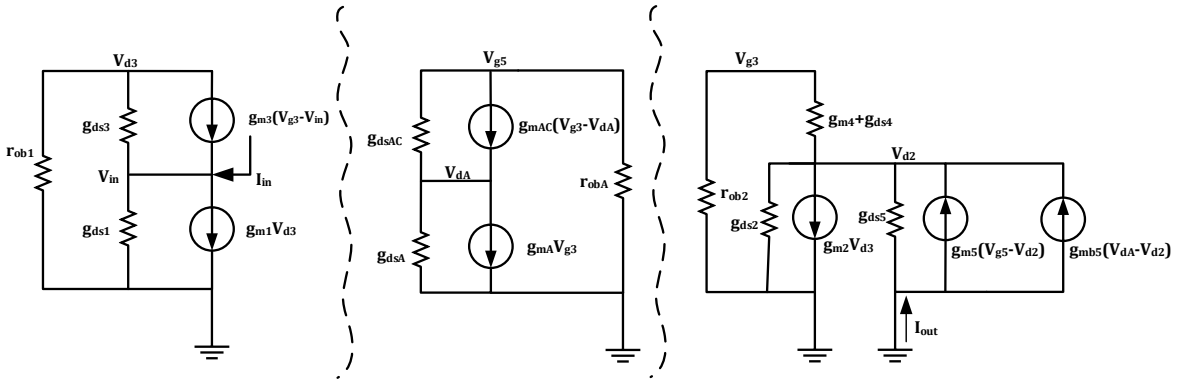


Fig 7. Small signal view of current mirror with proposed idea

$$R_{\text{in}} = \frac{V_{in}}{I_{in}}$$

$$= \frac{1}{\left[\left(g_{m1} + \frac{g_{m3}g_{m1}}{(g_{m5}+g_{mb5})(1+A)}\right) \times K + G\right]} \quad (10)$$

K and G in above equation are:

$$K = \frac{g_{m3}^2(g_{m5}+g_{mb5})(1+A)}{(g_{m5}+g_{mb5})g_{ds1}g_{ds3}(1+A) - g_{m1}g_{m3}^2}$$

$$G = g_{ds1} + g_{m3} + g_{ds3}$$

On the other hand, input resistance calculation of the circuit shown in Fig. 5 is reported (Azhari et al, 2011):

$$R_{in} = \frac{g_{m1}g_{ds3}g_{ds1}(A+1) - g_{m1}g_{m3}^2}{g_{m1}g_{m3}^2 g_{m5}(1+A)} \quad (11)$$

Nevertheless, precise input resistance calculation of the circuit shown in Fig. 5 results:

$$R_{\text{in}} = \frac{1}{\left(g_{m1} + \frac{g_{m3}g_{m1}}{g_{m5}(1+A)}\right)\left(\frac{g_{m3}^2 g_{m5}(1+A)}{g_{m5}g_{ds1}g_{ds3}(1+A) - g_{m1}g_{m3}^2}\right) + G} \quad (12)$$

Consequently, comparison of (10) and (12) shows that proposed idea has no change in the input resistance. The new circuit has low input impedance subsequently.

D. Current transfer analysis

Current transfer accuracy in current mirror design is one of the most significant factors. The best current mirror is one that has less current transfer error. For evaluating and analysis of this factor, following equations are calculated through small signal model of circuit as shown in Fig. 7.

$$I_{in} = V_{d3}(g_{m1} - g_{ds3}) + V_{in}(g_{ds1} + g_{m3} + g_{ds3}) - g_{m3}V_{g3}$$

$$V_{g3} = \frac{I_{out}}{(g_{mb5}+g_{m5})(1+g_{mA}r_{obA})}$$

$$V_{d3} = \frac{I_{out}}{g_{m2}}$$

$$I_{in} = \frac{I_{out}}{g_{m2}} \times g_{m1} + \frac{g_{ds1}}{g_{m1}g_{m2}}(g_{ds3} + g_{ob1})I_{out} + V_{g3}g_{ds1} + \frac{g_{m3}(g_{ds3} + g_{ob1})I_{out}}{g_{m1}g_{m2}}$$

$$\lambda = \frac{I_{out}}{I_{in}} = \frac{1}{1 + \frac{g_{ds1}}{(g_{m5} + g_{mb5})g_{mA}r_{obA}}} \quad (13)$$

It is clear from comparison of the calculated λ in (13) and the circuit shown in Fig. 5 (Azhari et al, 2011) which this idea has better accuracy in current transfer rather than the current mirror circuit shown in Fig. 5. The reason is that, according to (13), when the effective gm of the transistor M5 increases, the deduction $\frac{g_{ds1}}{(g_{m5}+g_{mb5})g_{mA}r_{obA}}$ becomes lower and will be less effective when sum with 1, therefore the value of λ will be closer to the ideal one.

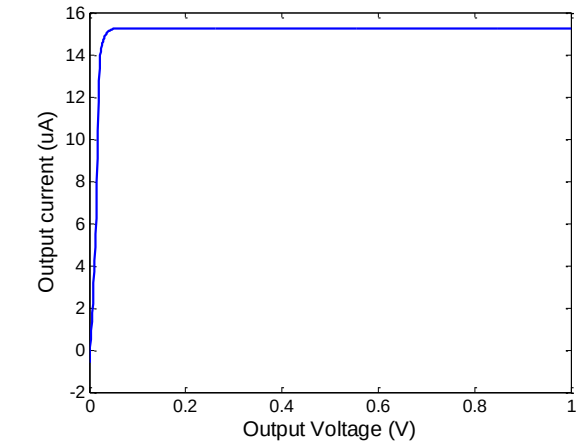
Simulation results

LVLP current mirror circuit with applied technique is simulated in 0.18 μm technology. To compare the results of improved current mirror with proposed circuit in (Azhari et al, 2011), power supply is set 1V and load resistance equal to 3kΩ. As well as, to evaluate the effect of improvement, all values of the circuit parameters are the same as to the values reported in (Azhari et al, 2011), just new signal path is added to bulk of M5. The simulation results of LVLP current mirror with and without applied technique are reported in the following.

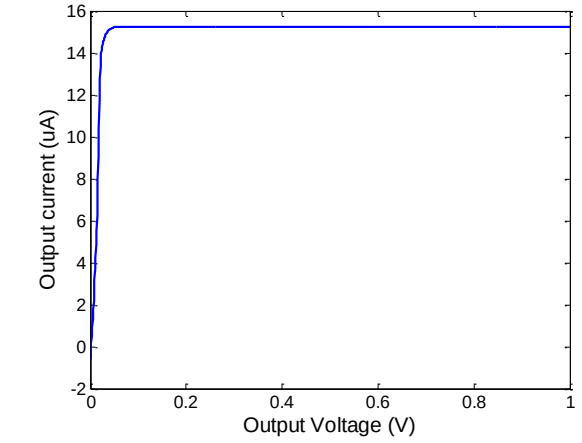
To find the output resistance of current mirror from simulation graphs, reverse slope of the output current versus output voltage curve, is measured. Fig. 8 (a) and (b) show the output current versus output voltage of current mirror with and without applied technique, respectively. As shown in Fig. 8 (a), the improved circuit exhibits extremely high output resistance of 39.5 GΩ, which results more than 5GΩ improvement Compare with the output resistor of current mirror without applied technique is reported in (Azhari et al, 2011) , (Fig. 8 (c)).

According to the results of simulation, minimum output voltage of both current mirrors, with and without applied technique, are 0.55 mV and show that dynamic range are same in both case.

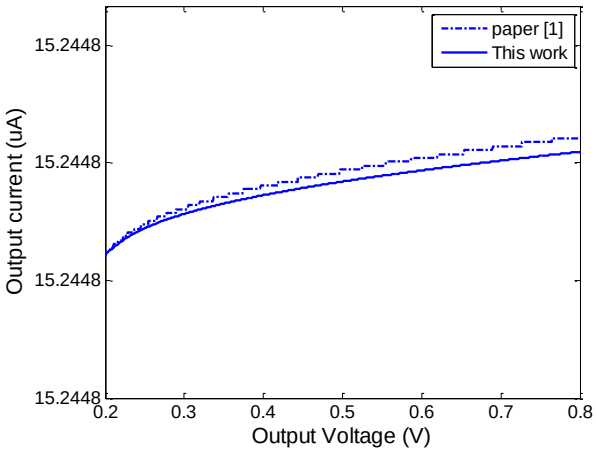
Fig. 9 belongs to output current versus output voltage for input current value of: 0 uA, 10 uA, 20 uA, 30 uA, and 40 uA. The results proved that proposed idea has no negative effect on circuit performances. As it is obvious from simulation results, proposed idea has the higher output resistance rather than other same reported works.



(a)



(b)



(c)

Fig 8. I_{out} versus V_{out} to find $g_{out}(R_{out}^{-1})$ for Current mirror circuit a) with b) without applied technique (Azhari et al, 2011), c) compare g_{out} of (a) and (b).

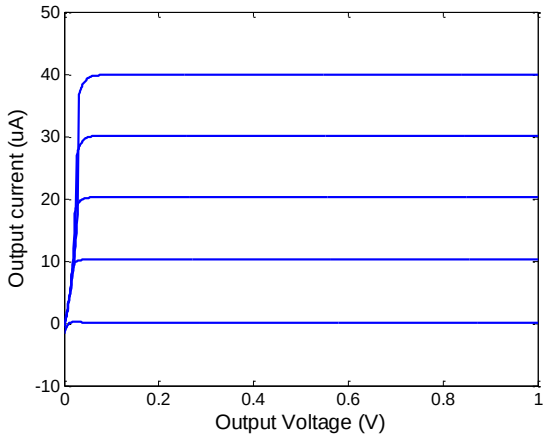
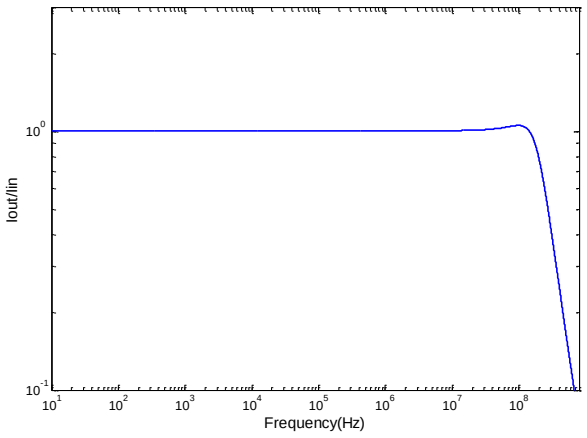


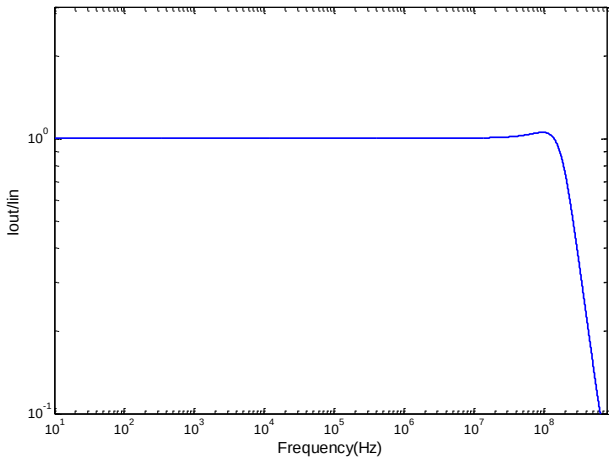
Fig 9. Output current versus output voltage for different input current of current mirror circuit with applied technique.

The frequency response of both current mirrors are illustrated in Fig. 10. As expected, not only did the applied technique have no negative impact on bandwidth, but also it made a little enhancement in circuit bandwidth. The bandwidth is achieved 216 MHz in this work. Input resistance versus frequency is depicted in Fig. 11. Result of simulation shows that input resistor is equal to 12.8 Ω. As expected, applied technique has no considerable effect on input resistance. The output current and input voltage versus input current are shown in Figs. 12 and 13, respectively. It is clear that current gain and input voltage are same in both case and has no considerable differences.

Comparative results of two current mirrors, with applied technique proposed in this work and without applied technique (Azhari et al, 2011), are summarized in Table 1. It should be noted that the difference between these two works is just extra signal path to bulk of M5, and all other things are completely same. As a result, the proof of which are independent of the parameters values and circuit design, using the applied bulk driven technique improve the current mirror performances.



(a)



(b)

Fig 10. Current mirror frequency response a) with b) without applied technique (Azhari et al, 2011)

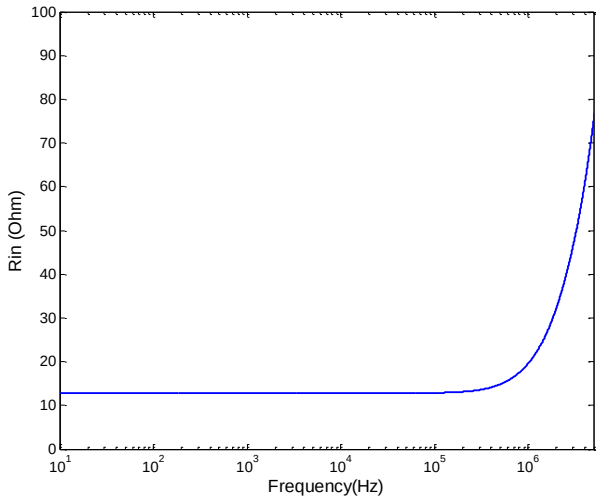


Fig 11. Input resistor of current mirror with applied technique

reference	(Azhari et al 2011)	(Raj et al 2015)	(Raj et al 2014)	(Bhawna et al 2014)	This work
I_{in} (uA)	15	0-250	0-700	0-280uA	**15**
I_b (mA)	5	NA	65	NA	**5**
$V_{in,min}$ (V)	0.058	NA	NA	NA	**0.058**
$V_{out,min}$ (V)	0.055	NA	NA	NA	**0.055**
R_{in} (Ω)	13.3	240	160	2730	**12.8**
R_{out} (Ω)	34.3 G	19.5G	8.55G	578K	**39.5 G**
BW (MHz)	210	285	4000	132	**216**
P (uW)	42.5	349	840	NA	**42.5**
V supply (V)	1	0.2	0.5	±0.5	**1**
Technology	0.18 um	0.18 um	0.35 um	0.25 um	**0.18 um**

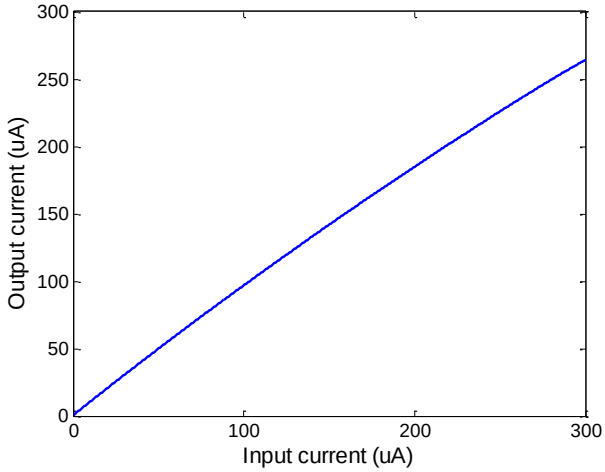


Fig 12. Output current versus input current for Current mirror circuit with applied technique.

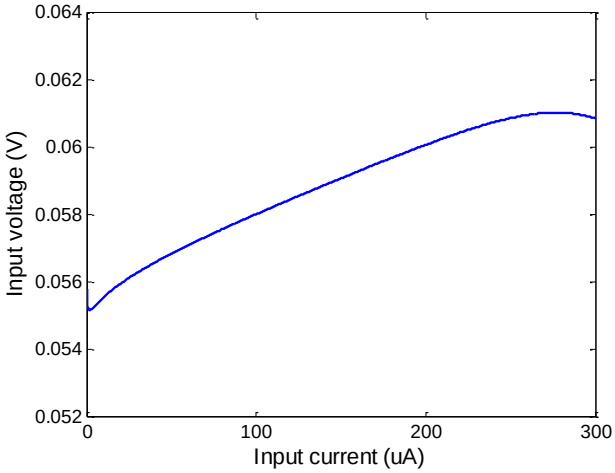


Fig 13. Input voltage versus input current for Current mirror circuit with applied technique.

Conclusion

This paper presents an LVLP current mirror with very high output resistance which is based on bulk driven technique. By using of an extra signal path to the bulk terminal of output transistor, the performance of current mirror, especially the output resistance, enhanced significantly. Simulation results show a significant output resistance improvement, which indicates more than 5GΩ improvement in compare with output resistor of the current mirror without applied technique. Also, this paper proved that appropriate use of bulk driven technique, independent of the parameters values and circuit design, is a suitable way to improve current mirror performance.

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