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Comparing and Modeling Statistical Variations on Stability of Nano-Transistors in 6T and 8T SRAM cells

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Abstract— **High statistical variation of static random access memory (SRAM) cell by Nano-transistors in combination with high density causes some memory performance problems. Therefore, presenting an accurate statistical model is one of the key issues in designing of SRAM memory. This article analyzes sensitivity of static noise margin (SNM) with different statistical variations in 6-transistors (6T) and 8-transistors (8T) SRAM cells and compares stability of 6T and 8T SRAM transistor cells. This article examines the effect of four samples of different variations on the statistical stability of 6T and 8T cells including: 1-threshold voltage variations, 2- supply voltage variations, 3-variations in width and length of the driver transistors and 4-word line voltage variations. In all the examined variations, in 8T SRAM cell, the SNM was higher than the 6T SRAM cell.**

Keywords-SRAM; static noise margin; SNM; variation.

I. INTRODUCTION

Statistical variation is intensified by scaling down dimensions of transistors in advanced technologies. Therefore, statistical variation analysis is a vital issue in achieving proper circuit performance [1-5]. The impact of these changes on SRAM cell transistors causes destructive defects and stability deficiencies, which do not completely damage cells. However, a rotational mode never merely appears under certain conditions and the cells are referred to as *"weak cells"* with insufficient noise margin due to such deficiencies [5-8]. This article uses a new method for SNM of a cell in response to statistical variations. This method use Monte Carlo simulation which it has highly accurate by BSIM4 models, which are extracted from numerical simulation device, and it have quantum physics constraints. In this method, as the flow chart of Fig. 1 shows, 1000 N-type and P-type simple transistors in BSIM4 model and by length of 35nm, with a unique structure of statistical changes resources including line-edge-roughness (LER), random-dopant-fluctuation (RDF) and poly-gate granularity (PGG), are replaced by SRAM cell transistors. In fact, 1000 random Netlist files were created for HSPICE simulator and each file is a SRAM cell with unique structure of intrinsic parameters. A SNM was extracted for any SNM file, which enables us to analyze mean of SNM, first torque (standard deviation), second torque (skewness), and examine SNM.

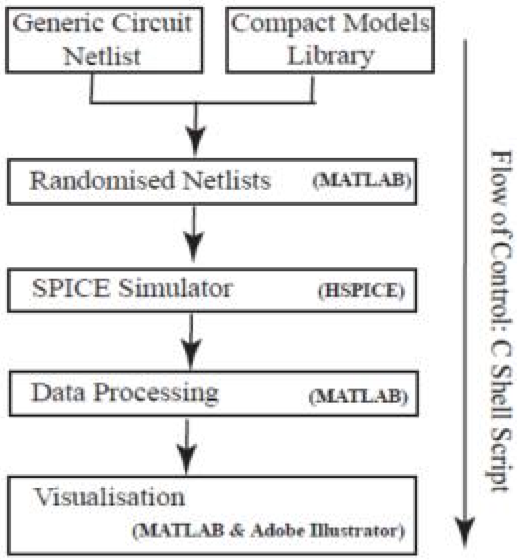

Figure 1. Example of a figure caption. (figure caption)

As shown in Fig. 2, an SRAM 6T cell is made of two reciprocally connected inverters and two access transistors. M_1 and M_2 are the driver transistors with the maximum role in maintaining data in a cell. M_3 and M_4 are the pull-up transistors which are used as a load for M_1 and M_2. M_5 and M_6 are the access transistors, which are responsible for reading data from a cell and writing data in a cell.

As Fig. 3 shows, the 8T SRAM cell is similar to the 6T cell with M7 and M8 transistors, which were added, and it makes access type to data in this cell different from the 6T cell [8-11].

This paper is arranged as follows: in section II, the threshold voltage variations are presented. Supply voltage variations are described in section III. In sections IV and IIV, variations of the size of the driver transistors and word line voltage are presented, respectively. Some conclusions are described in last section.

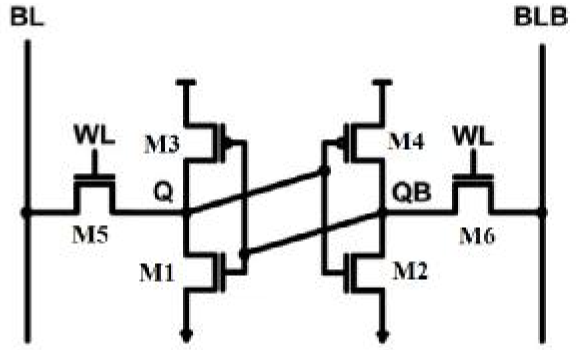

Figure 2. The 6T standard SRAM cell

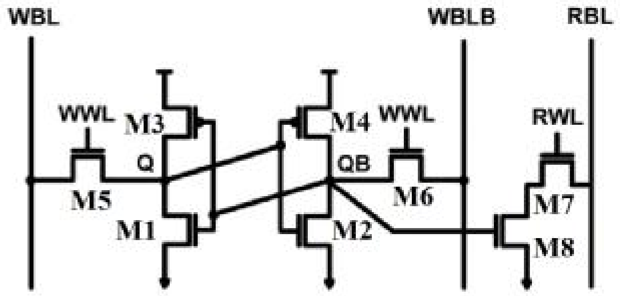

Figure 3. The 8T SRAM cell

II. Threshold Voltage Variations

Some of the changes are random, which can only be expressed using their statistical distribution. This is a notable point in designing Nano-scale ICs and one of the major constraint coefficients of circuit performance and its reliability. Random variations sources (RDF, LER, and PGG) are as the major sources of threshold voltage changes for the transistor with the channel lengths smaller than 40 nm [8].

Variations in threshold voltage (V_{TH}) of driver transistors have the greatest impact on the stability of cells, which is caused by greater proportion of $\frac{W}{L}$ as compared with other cell transistors. V_{TH} of driver transistors reduces with increased bulk-source voltage (V_{BS}). Non-destructive maintenance condition of a SRAM cell increases leakage flow of this transistor and enhances stability. Increased V_{BS} in access transistors reduces VTH of the transistor and makes easy access to a cell. For this reason, access transistors and load are shunted strongly in each cell accessed for reading and writing data. They expose the low mode of a cell to a destructive effect [9].

Figure 4 shows SNM standard deviation for variations in V_{TH} of driver transistors in both cells. As type of access to the cell is different in 8T cell, its stability exceeds 6T cell and the variations in V_{TH} of access transistors has fewer effects on cell stability. As access to data only depends on two access transistors in the 6T cell, variations in V_{TH} of access transistors cause further deviation as compared with 8T cell in cell stability. Figure 5 shows the standard deviation in which deviation in V_{TH} of driver transistors of cell 8T (65%) and access transistors in this cell (15%) respectively cause the maximum and minimum deviation in the second torque of SNM.

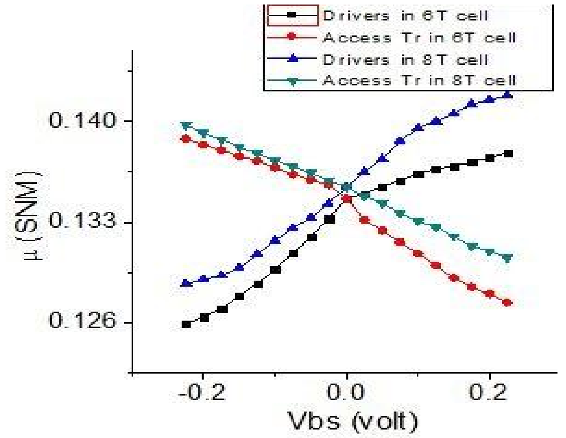

Figure 4. SNM standard deviation for variations in V_{TH} of driver transistors in 6T and 8T SRAM cells

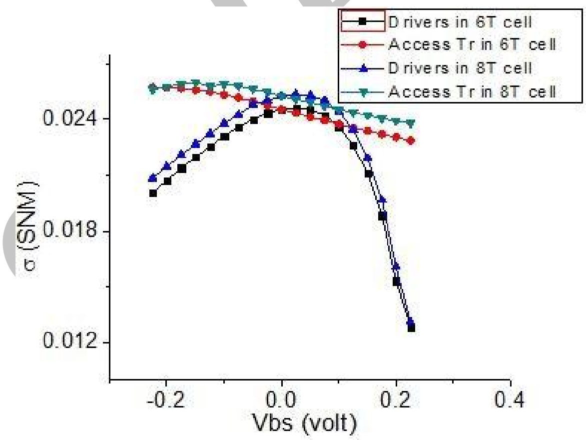

Figure 5. The maximum and minimum deviation in the second torque of SNM for 6T and 8T SRAM cells.

Figures 6 and 7 compares SNM distribution with 40% deviation in V_{TH} of access transistors in 8T and 6T cells and show superiority of 8T cell to 6T cell in data stability.

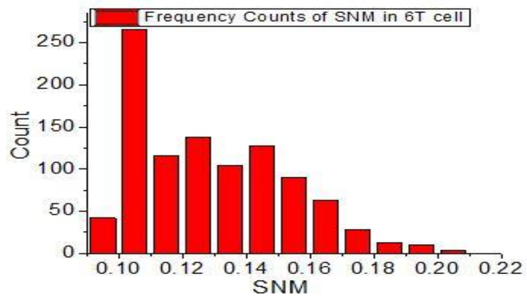

Figure 6. The SNM distribution with 40% deviation in V_{TH} of access transistors in 6T SRAM cell

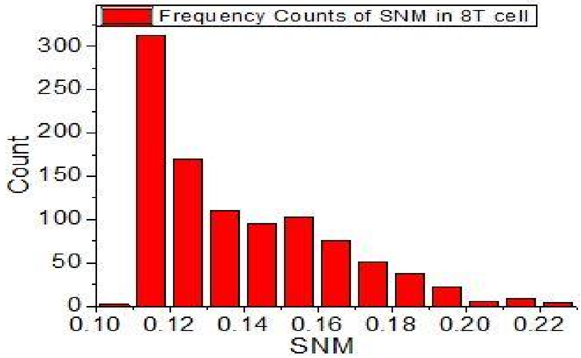

Figure 7. The SNM distribution with 40% deviation in V_{TH} of access transistors in 8T SRAM cell

III. Supply Variations

These variations are resulted from supply networks and surrounding environment noise. Supply voltage variations assume an error through the supply voltage network of an SRAM cell. SNM shows a strong dependency on cell supply variations, as word line voltage and global bit lines in V_{DD} are complete. This makes an access transistor shunt pull-up transistors strongly and affect the cell's low mode in a destructive manner [10]. As Fig. 8 shows, supply voltage variations have a considerable effect on SNM standard deviation, and SNM deviations in 6T cell exceed 8T cell. In the standard deviation of Fig. 9, supply deviations in the 8T cell have a further effect on the second torque of SNM as compared with the 6T cell.

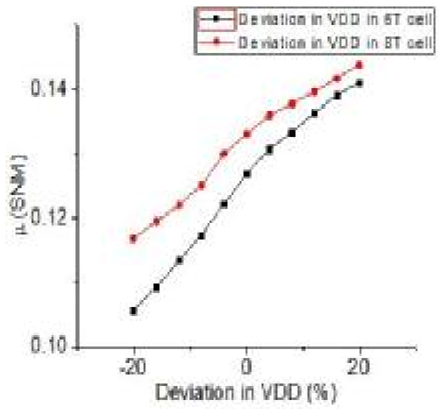

Figure 8. Supply voltage variations effect on SNM standard deviation in 6T and 8T SRAM cells.

Gradient of variations in the third torque in fig. 10 is relatively equal in both cells and such a similarity of gradient is because of the difference of both cells in type of access to data. In this condition, both cells are accessed for reading, word line voltage and global bit lines in V_{DD} are complete, and variation only occurs in supply of the two inverters, which connect reciprocally and preserve data. As Figs 11 and 12 shows, SNM distribution for 15% of variation in supplying both cells, 8T cell has a higher SNM.

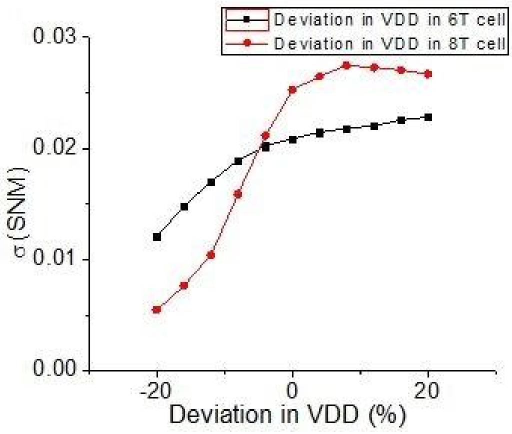

Figure 9. The SNM distribution with ±20 % deviation in supply voltage in 6T and 8T SRAM cells

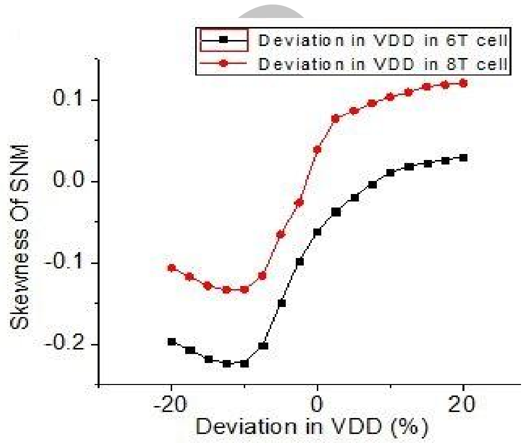

Figure 10. Gradient of variations in the third torque for 6T and 8T SRAM cells

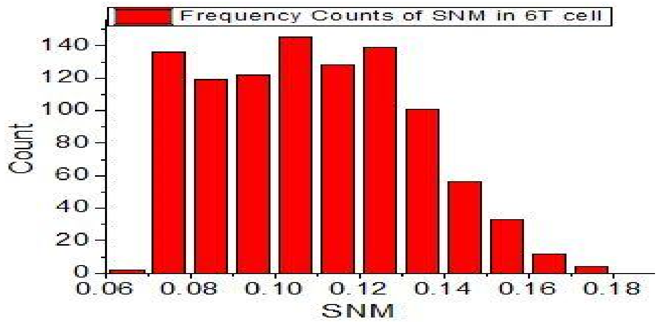

Figure 11. The SNM distribution with 15% deviation in supply voltage in 6T SRAM cell

I. Vauriation in Proportion Driver Transistors

To assure non-destructive reading, sufficient noise margin, and preservation of a reasonable SNM and efficiency in SRAMs of following large CMOS, cell ratios should increase from the usual rate of $\frac{W}{L}Driver = \frac{W}{L}Access = 2$ to higher ratios in order to preserve scaling balance and advantage of deep multiten-nanometer technologies [10]. Due to higher $\frac{W}{L}$ ratio of driver transistors to other transistors, we only study the effect of variations in $\frac{W}{L}$ ratio of the transistors on SNM and the two cells.

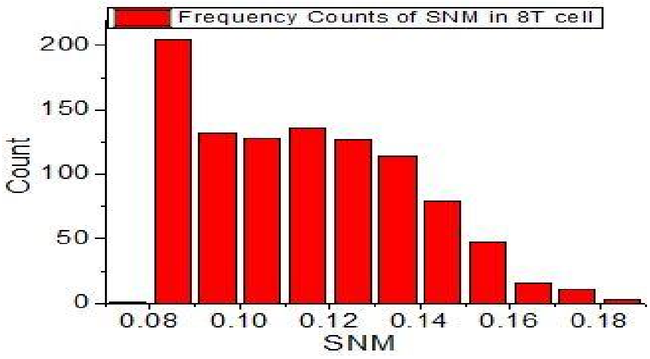

Figure 12. The SNM distribution with 15% deviation in supply voltage tin 8T SRAM cell

Figure 13 shows the dependency of SNM for 6T and 8T SRAM cells on W_{eff} and L_{eff} variations of driver transistors. SNM reduction is considerable when the effective changes of length and width of a transistor remain 20% of the typical values. Analysis of Fig. 13 shows that the 8T cell is more stable than the 6T cell and with W increasing from a typical value in both cells, cell ratio increases and leads to SNM improvement. With the L of driver transistors increasing in the cells, cell ratio decreases and it reduces SNM.

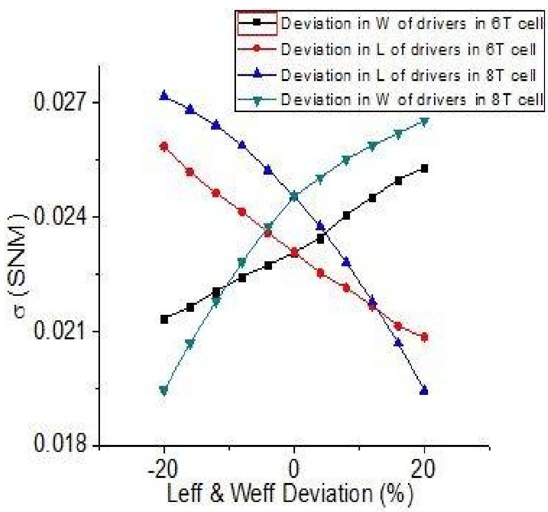

Figure 13. Dependency of SNM for 6T and 8T SRAM cells on W_{eff} and L_{eff} variations of driver transistors

The standard deviation in Fig. 14 shows that the variations in $\frac{W}{L}$ ratio of 8T cell cause further deviation in the second torque of SNM. Figure 15 shows skewness and SNM for variations in   ratio of both cells in which gradient and variation ratio of both cells are almost equal. Fig. 16 and fig. 17 show SNM distribution for 20% reduction in L of driver transistors in both cells, which indicates higher noise margin of 8T cell.

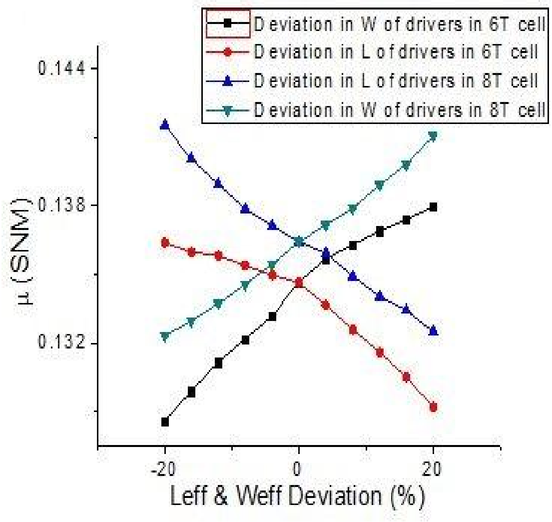

Figure 14. The 20% variations in $\frac{W}{L}$ ratio of driver transistors in 6T and 8T SRAM cell

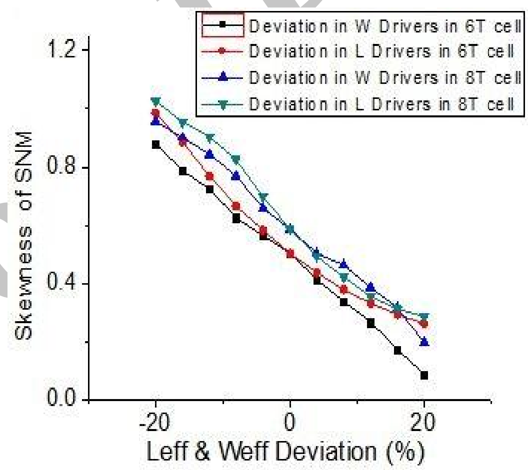

Figure 15. Gradient and variation ratio of 6T and 8T SRAM cells due to skewness and SNM by ± 20% variations in effective $\frac{W}{L}$ ratio

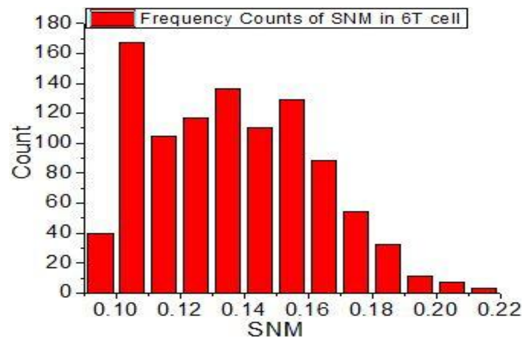

Figure 16. The SNM distribution for 20% reduction in L of driver transistors for 6T SRAM cell

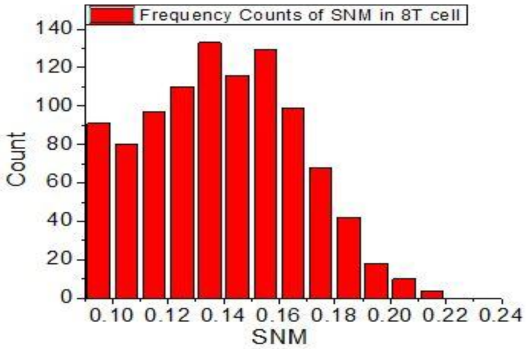

Figure 17. The SNM distribution for 20% reduction in L of driver transistors for 8T SRAM cell

II. WORD LINE VOLTAGE VARIATION

If word line voltage (V_{WL}) be lesser than threshod voltage of access transistor, it has no effect on SNM and it is an isolation cell of read and write drivers. If V_{WL} be bigger than threshod voltage of access transistor, the cell is accessed for reading or writing, and access transistors start shunting load transistors and lifting the node that saves low mode and reducing SNM considerably [11]. As Fig. 18 shows, the dependency of SNM on voltage variations of word line voltage for 6T and 8T cells, 8T cell has a higher noise margin and with the increased voltage in both cells, SNM decreases considerably.

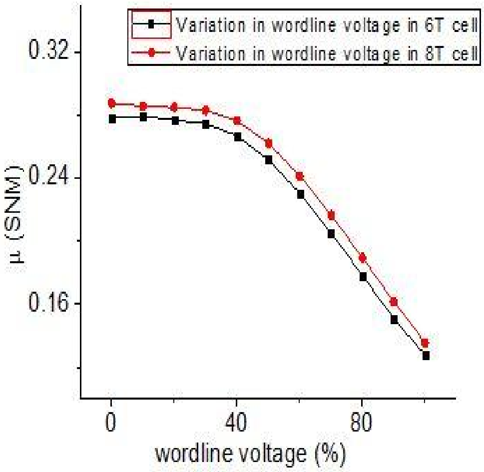

Figure 18. Dependency of SNM on voltage variations of word line voltage for 6T and 8T SRAM cells

It is observed in the standard deviation of Fig. 19 and the second torque of SNM of Fig. 20 that the maximum deviation occurs in 60% of the typical value of voltage (Vwl) in which the threshold voltage of access transistors and the cell is accessed for reading and writing.

Figure 21 and fig. 22 show SNM distribution while the voltage (Vwl) is in 60% of its typical value in each cell, which indicates superiority of 8T cell over 6T cell as far as stability is concerned.

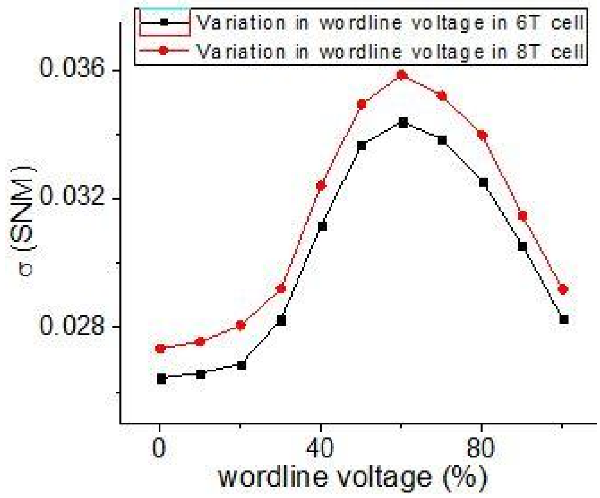

Figure 19. The standard deviation in word line voltage for 6T and 8T SRAM cells

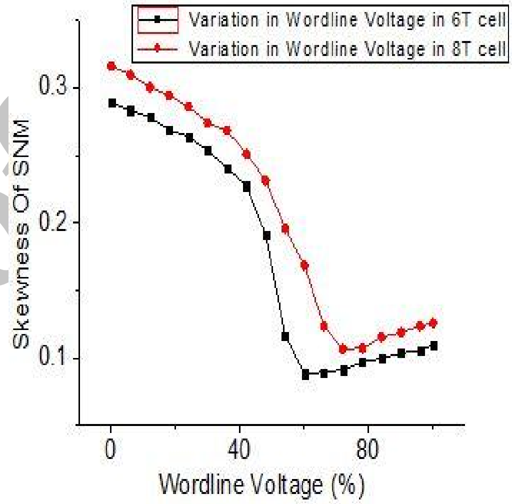

Figure 20. The second torque of SNM in 6T and 8T SRAM cells

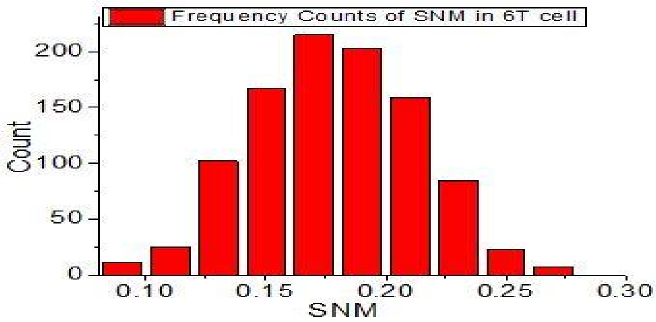

Figure 21. The SNM distribution with 60% deviation in word line voltage for 6T SRAM cell

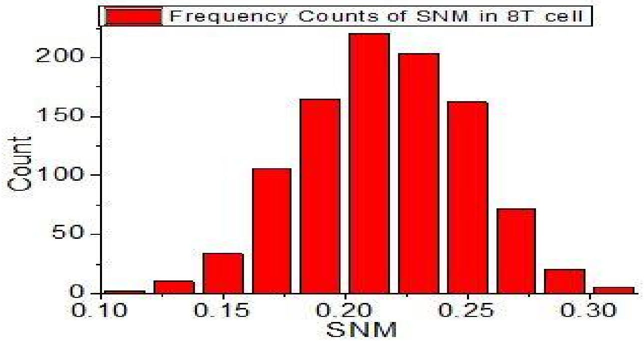

Figure 22. The SNM distribution with 60% deviation in word line voltage for 8T SRAM cell

III. CONCLUSION

With respect to technological advancements and increase of random variations, manufacturing ICs without considering statistical variations is a waste of time and money. Therefore, results of these variations may help informed design based on statistical variations. Stability of SRAM cells determines design, manufacture, and test. Therefore, broad analysis of SNM sensitivity is a major parameter in identifying a weak cell with insufficient noise margin.

This article compared stability between 6T and 8T cells against different statistical variations. In all the examined variations, in 8T SRAM cell, the SNM was higher than the 6T SRAM cell as far as stability was concerned; however, as far as area and size were concerned, 6T cell circuit is superior as it had fewer transistors. Therefore, choosing each cell is an exchange between circuit size and SNM, which is used based on a target application.

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